Design and Hardware Overview of PUEO Rachel Scrandis for the PUEO Collaboration







PUEO's Science Goals





PUEO's goal is to use radio to measure (or set the best limits on) the UHE neutrino flux in order to understand the most extreme environments of our universe

Based off of ANITA heritage, it will leverage the Askaryan emission mechanism to measure these neutrinos

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PUEO's Science Signal





| ANITA-IV Recorded Data | a |
|------------------------|---|
| (O(10^7) events) | |

| Thermal Noise | ~99% of data |
|---------------------|---------------|
| Anthropogenic | ~0.9% of data |
| Cosmic Rays | ~30 events |
| Neutrino Candidates | ~a few events |
| A. Ludwig Thesis | |

Over 4 successful flights, ANITA saw 100s of UHECRs, no excess in neutrino-like events, & a few upward-going air shower candidates

1e-7

PUEO will improve on background rejection & trigger threshold to increase discovery potential for UHE neutrinos 3

PUEO Design



PUEO will be searching for impulsive radio signals in the 300-1200 MHz range and will be capable of reconstructing neutrino direction, energy, and potentially flavor

PUEO will feature:

- 96 quad-ridge horn antennas (192 RF channels)
- 8 sinuous low frequency antennas (16 RF channels)
- Phased array trigger
- Telemetry capabilities
- Navigation suite
- On board power system & housekeeping



Antennas





Custom antennas feature (in 300-1200 MHz band):

- Dual polarization
- <-10dB in return loss (S11)
- <-30dB in port isolation (S21)
- ~10dBi boresight gain (ANITA-IV gain: ~8dBi)

Characterization measurements and sims ongoing



RF Chain





Signal conditioning happens in 2 stages:

- Antenna Mounted Pre-Amplifier (AMPA) gives 1. ~40dB
- Octal Receiver (2nd stage amp) gives ~30dB

With cable losses, chain presents 68dB of gain & 23% lower noise temp (inherit chain noise) than ANITA-IV **Full Flight Chain**

Impulse Response (normalized)

Integrated Power (normalized)

30

--- 90% Power: 6.4 ns

30

--- 15 ns

Time (ns)

40

40

50

50

10

10

1.0

0.0

20

20



LF Instrument



LF Instrument will target lower frequency air showers (CRs and upgoing Taus). Antennas are sinuous design, sensitive to 50-300MHz.

- Conductive fabric (Nylon ripstop coated with Ni/CuAg) on polyester
- ~5dBi boresight gain and 30° beam width
- Will be stowed in gondola during launch, and deployed at float











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Work by Patrick Allison, Lucas Beaufore, Jim Beatty, Taylor Coakley, & Aera Jung

Sampling Unit for Radio Frequencies (SURF)

- Uses RFSoCs (x8 ADC @ 3GHz) to digitize 8 RF channels (8 antennas, one pol = 2 phi sectors)
- Conditions signal with FIR low pass filter (boost SNR), 2 biquad notch filters (satellite noise rejection), and 12-to-5 bit conversion (offset & gain control)
- On board FPGA handles beamforming & triggering:
 - L1 Trigger: 100kHz, beam forming with 2 phi sectors (1 SURF)
 - L2 Trigger: 100Hz, beam forming with 4 phi sectors (pulls from neighboring SURF)

Triggering Unit for Radio Frequencies (TURF)

- L3 Trigger: under design (CW elimination, polarization check, etc...)
- Communicates with SFC to record triggered data

Data Storage & Downlinking





Starlink used recently on balloon $_{PG}$ flights \rightarrow exploring use for PUEO (after mitigating RFI & thermal concerns)



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Work by Keith McBride, Cosmin Deaconu, Connor Godden, TsungChe Liu, Jiwoo Nam, & Natalie Orrantia

Triply redundant data storage onboard

- 2 HD enclosures (128TB of storage each)
- 1 SSD enclosure (80TB of storage)

Quick connect mounting/demounting for fast takeaway



Data downlinking rates dependant on what we decide to use:

- LOS EVTM (up to 12.8 Mbps or so)
- Iridium (255 bytes/every 15M)
- TDRS (6 kbps)
- Starlink (1-40 Mbps downlink)

Location & Orientation Tracking



ABX2: Differential GNSS 0.02° heading, 0.075° pitch/roll

Star Tracker:

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Mag <6 stars 0.001° heading, 0.001° pitch/roll

Sun Sensor: Sun 0.17° heading, ~0.3 ° pitch/roll



Power & Housekeeping



PV Array



Power comes from PV array \rightarrow designed to generate 1800W

• Power box supplies 24V, 12V, 5V, and 4V across payload

Housekeeping board also lives in power box

- Monitors power consumption across payload
- Monitors temperatures across payload
- Toggles on/off RF chain



Work by Brian Rauch, Keith McBride, and Zack Martin

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200ft LMR-240 to discone

monitoring antenna

50ft LMR-6

to HPol

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Work by Steven Prohira, Steph Wissel, Julien Alfaro, Shoukat Ali, Dave Besson, Kenny Couberly, Rob Young, & Andrew Zeolla

Field stations along PUEO path that pulse as payload flies

overhead

HiCaz, the azimuthal monitor. Lower PV are HPol (top)

and VPol (bottom) transmitting antennas.

Size-wise, similar to HC2 but with the addition of the VPol antenna

antenna PV dimensions subject to slight revision.

High-altitude Calibration

Small hand-launched balloons

that follow main payload



Upper PV contains

above upper PV is

electronics



Calibration Plan

Ground Calibration

Outlook





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Extra Slides

Full System Diagram





RF Chain Block Diagram





LF RF Chain





LF signal conditioning happens in two stages

- LF AMPA mounted directly behind antenna gives ~20dB
- LF Receiver gives ~55dB



Work by Daniel Washington

Flavor Reconstruction





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Phased Array Triggering





On board, preset arrival directions will be checked by applying relevant time delays and summing each channel in a sector

- If any of the beams (arrival directions) passes some voltage threshold, event will pass the trigger
- This beam forming + coherent summing (summing each channel) will help reject thermal noise triggers (SNR goes as $\sqrt{N(ant)}$)



Figure by Patrick Allison

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DAQ Block Diagram

Signal moves from right to left

LF digitizing and L1/L2 triggering happens on independent SURF, and speaks to the global trigger with an OR logic

TURFIO is between SURF and TURF; it synchronizes clocks, collects data, and buffers it





DAQ Hardware Specs



SURF: Trenz TE0835 with a Xilinx ZU47DR RFSoC

- FPGA Package: E1156 (35 x 35 mm)
- Engine: Quad-core Arm Cortex-A53 MPCore up to 1.3GHz
- 8 RFADCs with 4.096 GSPS

TURFIO: Xilinx Artix-7 FPGA

TURF: Xilinx Zynq Ultrascale+ MPSoC

Nav Suite Block Diagram





Power Block Diagram



