Fermilab

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CMS

Aug 8, 2025

Timing Detectors

Deep Dive, and perspectives from the CMS ETL

Murtaza Safdari
2nd Annual US Muon Collider Collaboration Meeting
Link to Indico

U.S. DEPARTMENT of ENERGY
Fermi National Accelerator Laboratory is managed by FermiForward for the U.S. Department of Energy Office of Science

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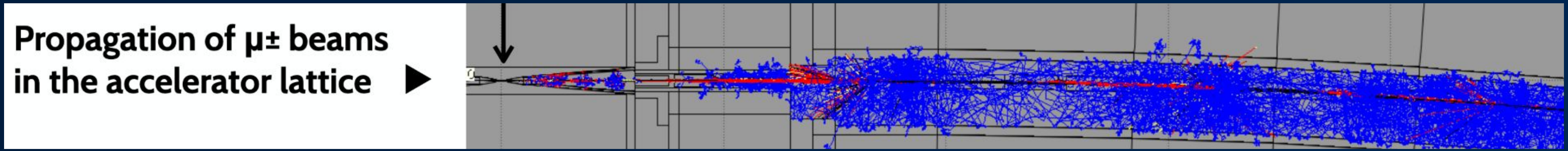
Case for Timing Detectors at Muon Colliders

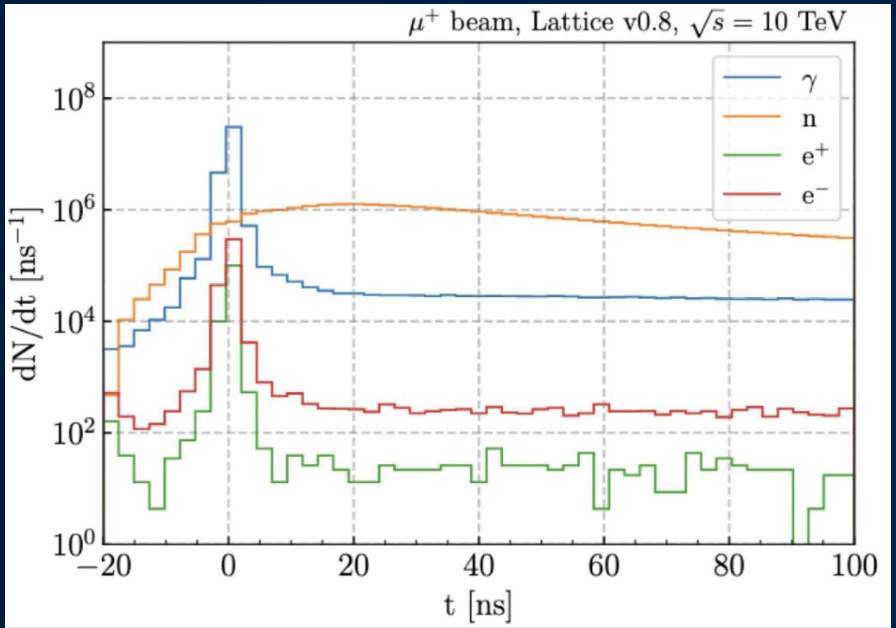
Beam Induced Background

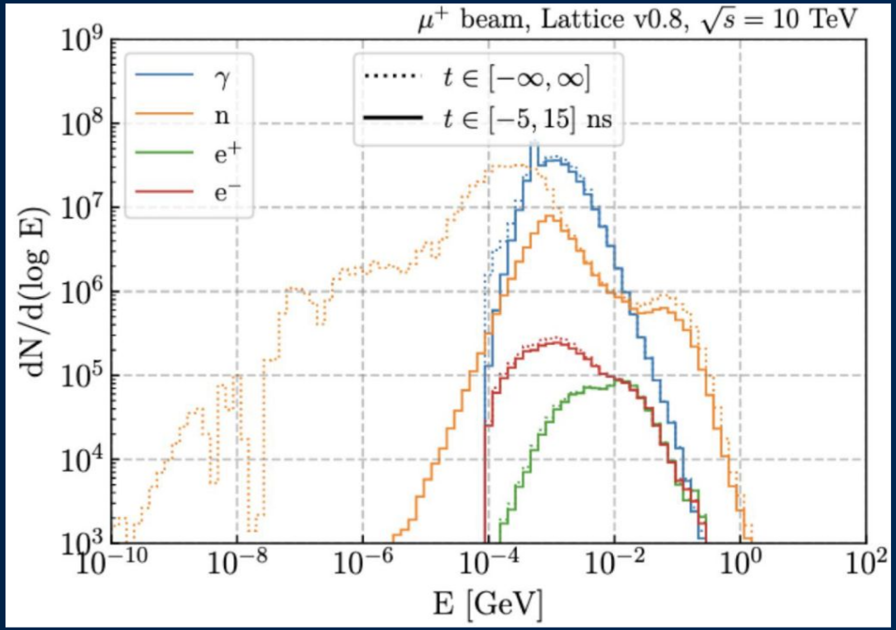
Primarily dealing with out-of-time background from muon decay products. Intense, continuous flux of low-energy photons, electrons, positrons, and neutrons that floods the detector

N. Bartosik



Kiley Kennedy at IMCC 2025





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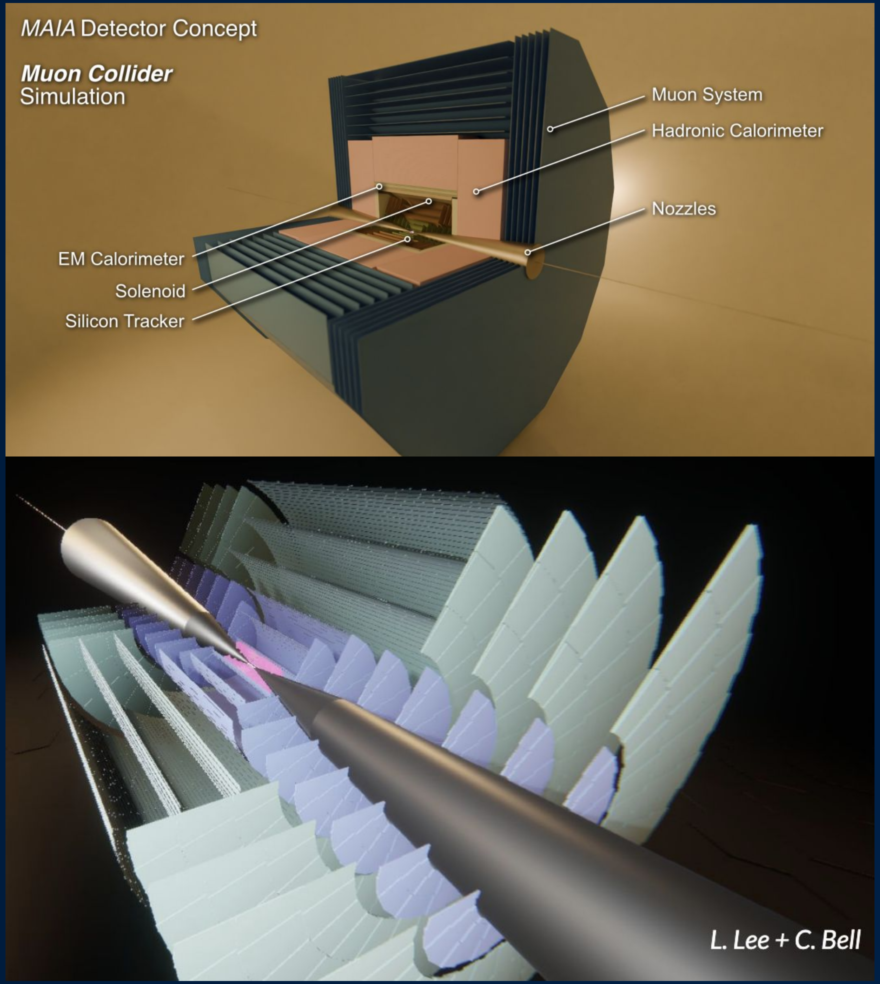
Precision timing for BIB & Physics

Snapshot from the *MAIA detector concept*



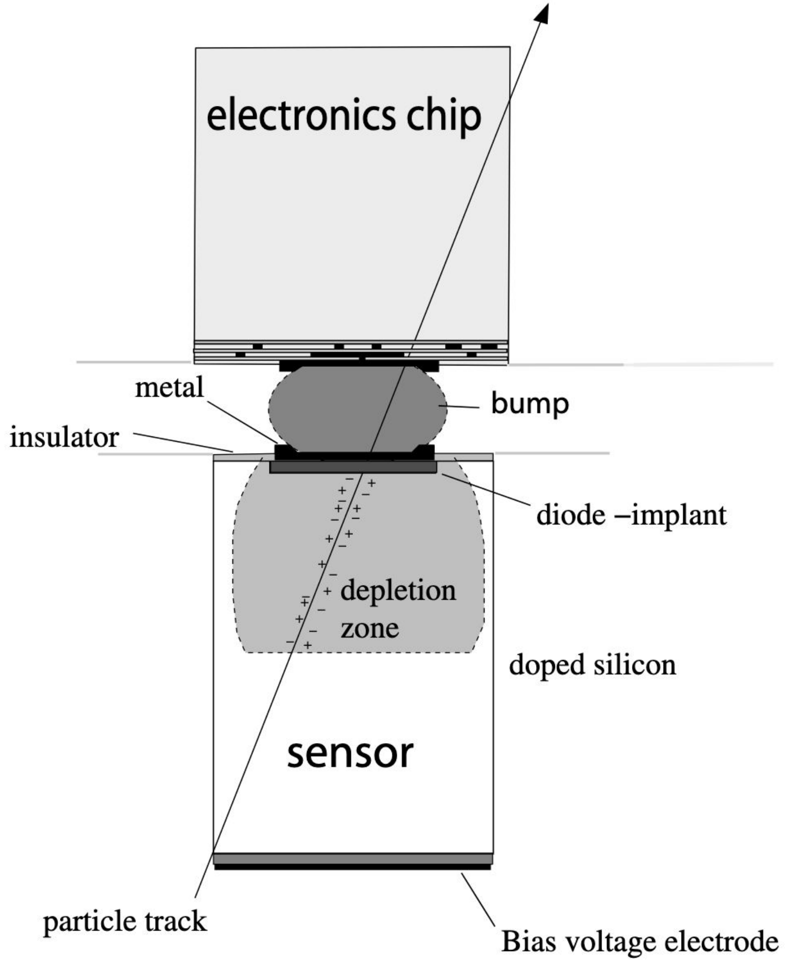
Kiley Kennedy at IMCC 2025

- Timing detectors / 4D tracking are essential for tackling BIB at muon colliders
- Also gain PID for low momenta particles with ToF
- LLP and displaced vertex tagging

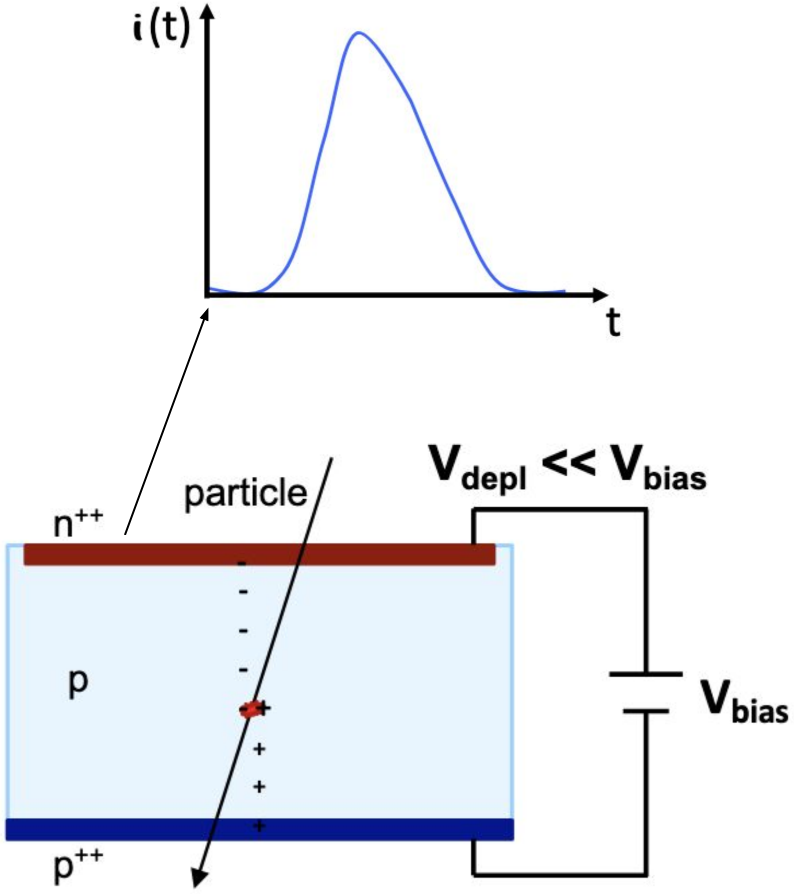
	Vertex Detector	Inner Tracker	Outer Tracker
Sensor type	pixels	macro-pixels	micro-strips
Barrel Layers	4	3	3
Endcap Layers (per side)	4	7	4
Cell Size	$25\,\mu m \times 25\,\mu m$	$50\,\mu m \times 1\,mm$	$50\,\mu m \times 10\,mm$
Sensor Thickness	$50\,\mu m$	$100\,\mu m$	$100\,\mu m$
Time Resolution	30 ps	60 ps	60 ps
Spatial Resolution	$5\,\mu m \times 5\,\mu m$	$7\,\mu m \times 90\,\mu m$	$7\,\mu m \times 90\,\mu m$

Fundamentals of a Timing Detector

Standard “Hybrid” Pixel Model



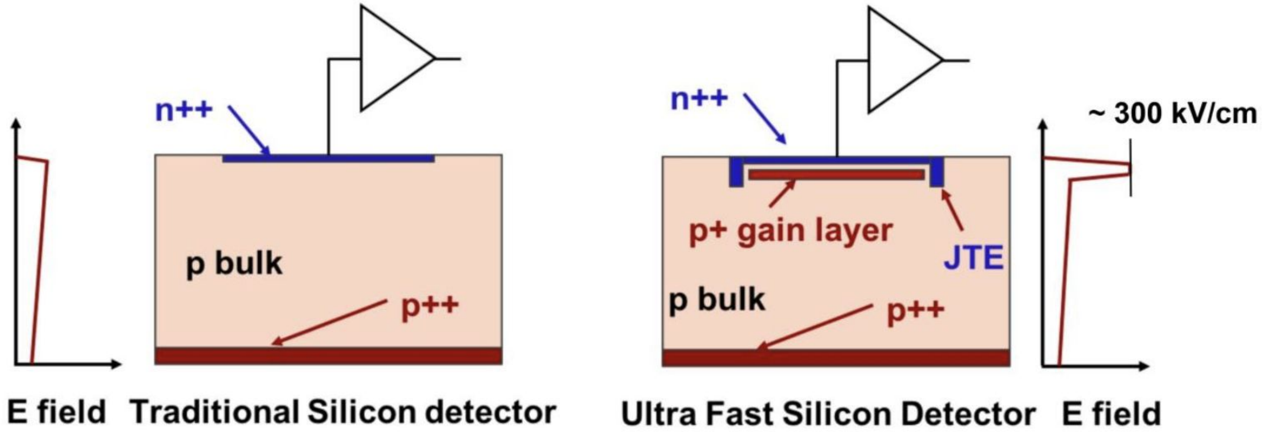
Pixel Detectors

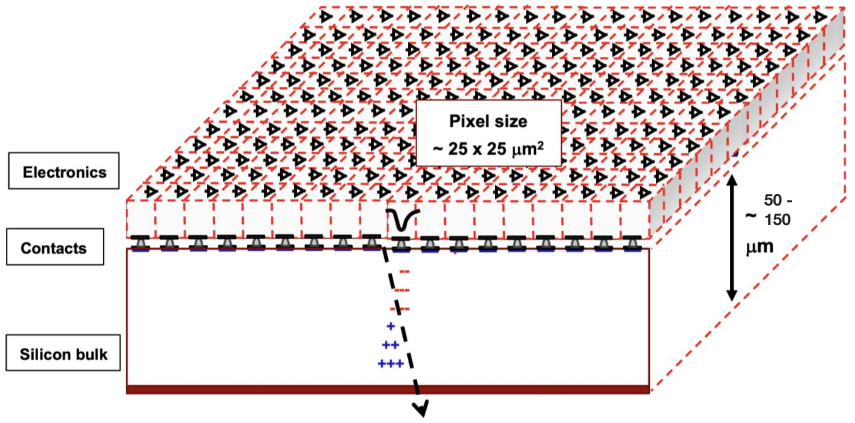


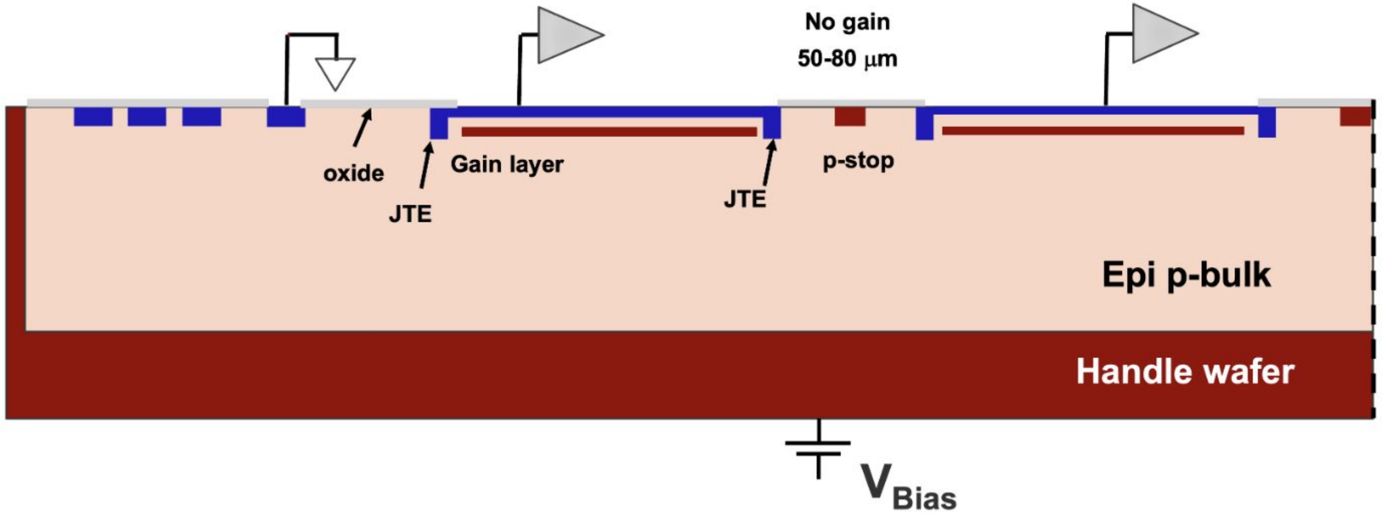
V Sola at VCI2025

Fundamentals of a Timing Detector

Standard “Hybrid” Pixel Model - Low Gain Avalanche Diode







N Cartiglia et al

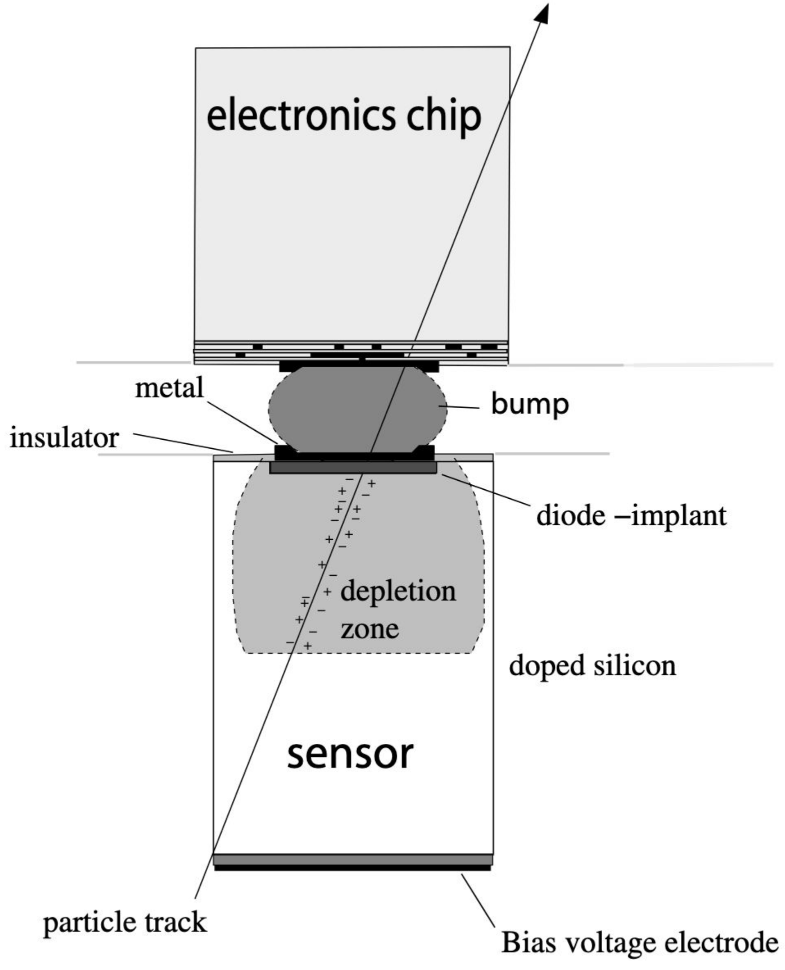
Low Gain Avalanche Detector (LGAD)

- n on p sensor with p-type mult. layer
- Low gain (G~10): improve signal slope
- Developed at CNM Barcelona
- Proposed for timing by UCSC/Torino

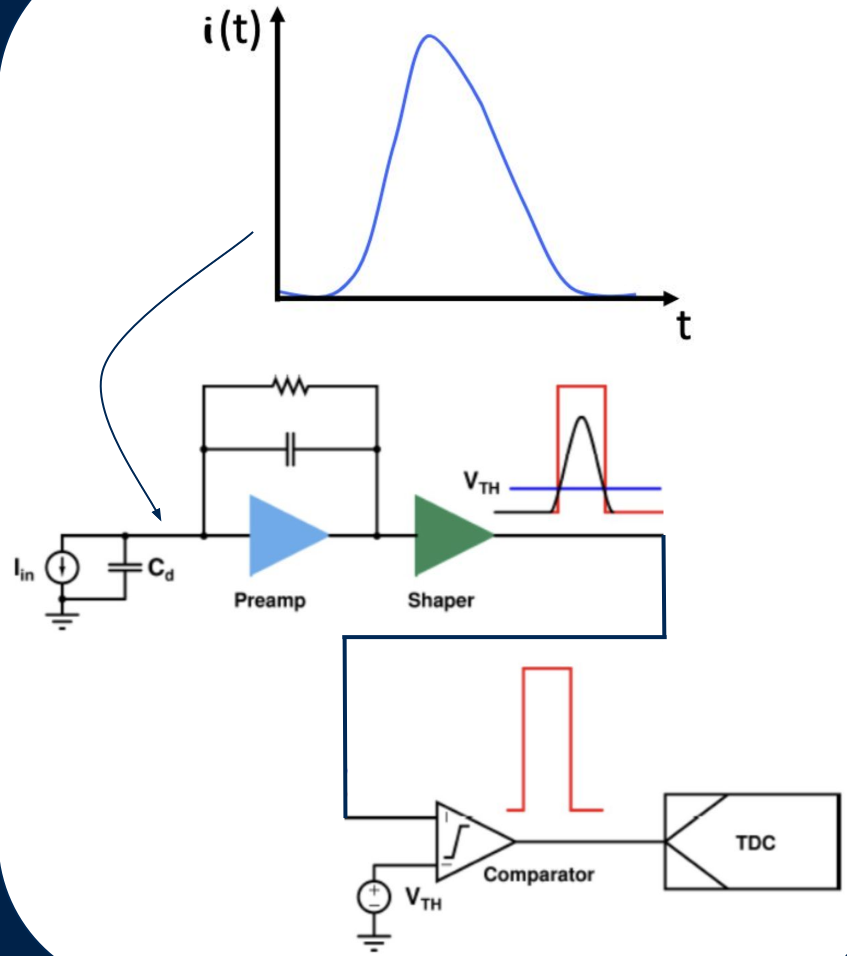
~15 year development cycle from idea to production in first-gen detectors

Fundamentals of a Timing Detector

Standard "Hybrid" Pixel Model - Readout Chain

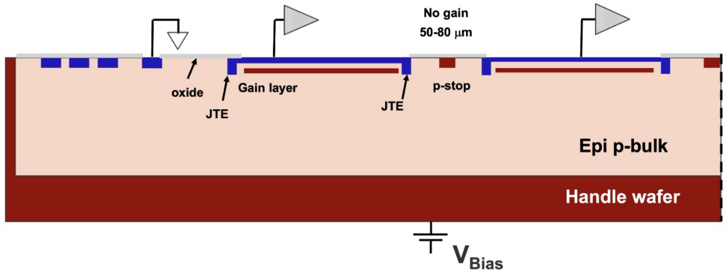


Pixel Detectors



Fundamentals of a Timing Detector

Standard “Hybrid” Pixel Model - Basics of Time Resolution



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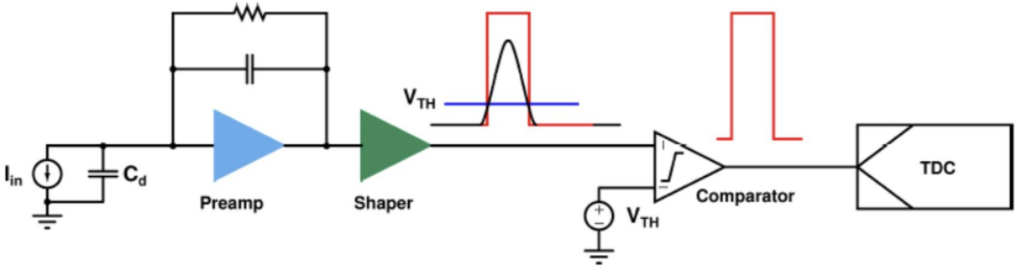
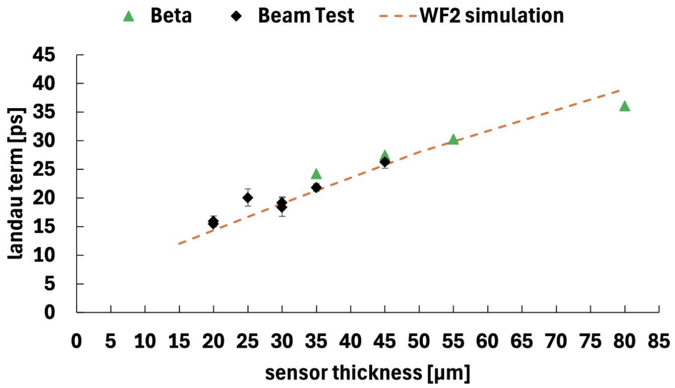
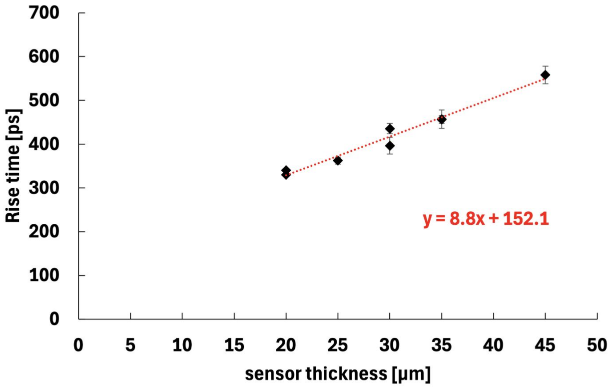


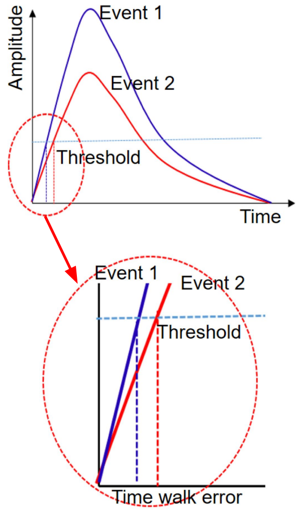
$$\sigma_t^2 = \sigma_{Landau}^2 + \sigma_{timewalk}^2 + \sigma_{jitter}^2 + \sigma_{TDC}^2 + \sigma_{clock}^2$$

V Sola at FAST2025





$$\frac{t_{rise}}{S/N}$$



Time Walk Effect

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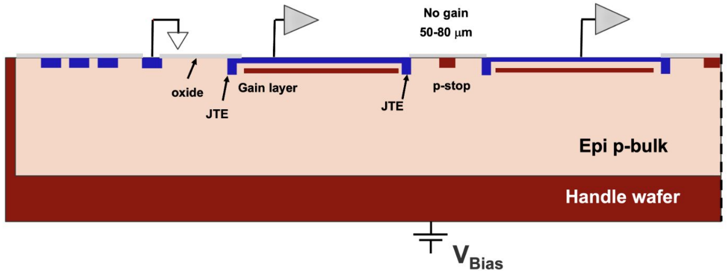
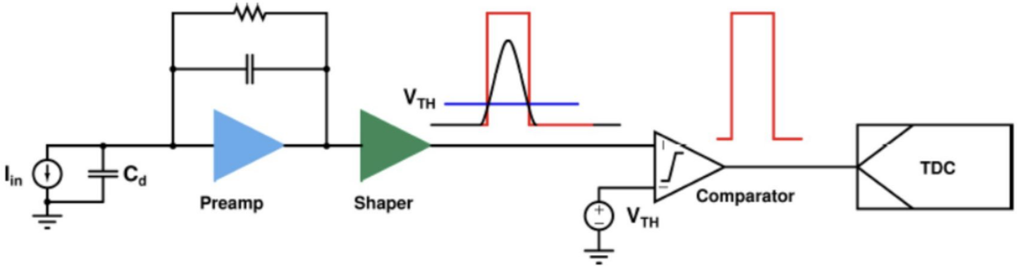
Fundamentals of a Timing Detector

Standard “Hybrid” Pixel Model - Basics of Time Resolution





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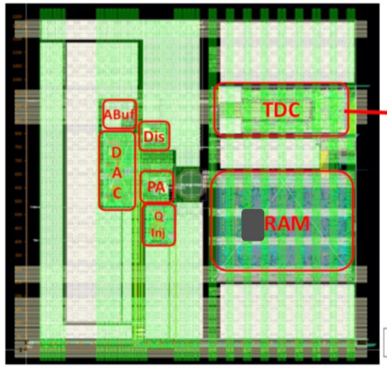
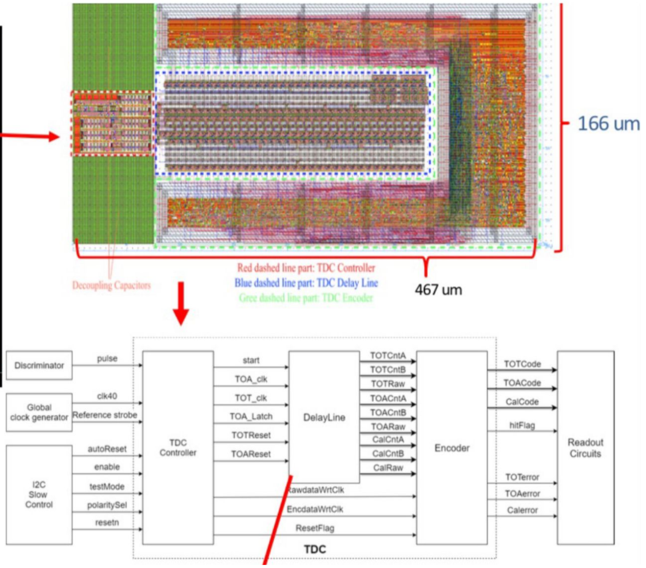
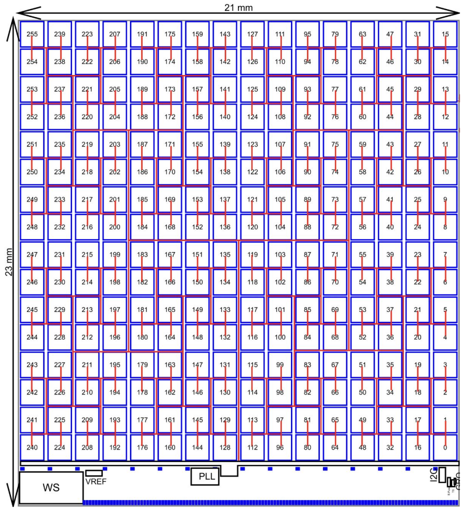
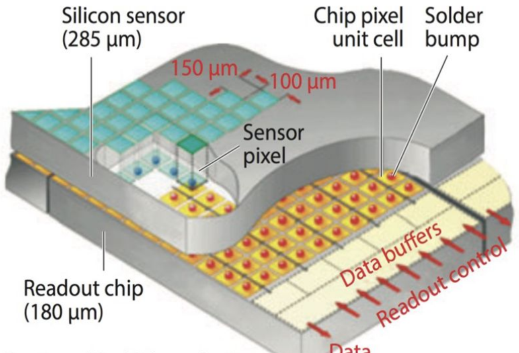




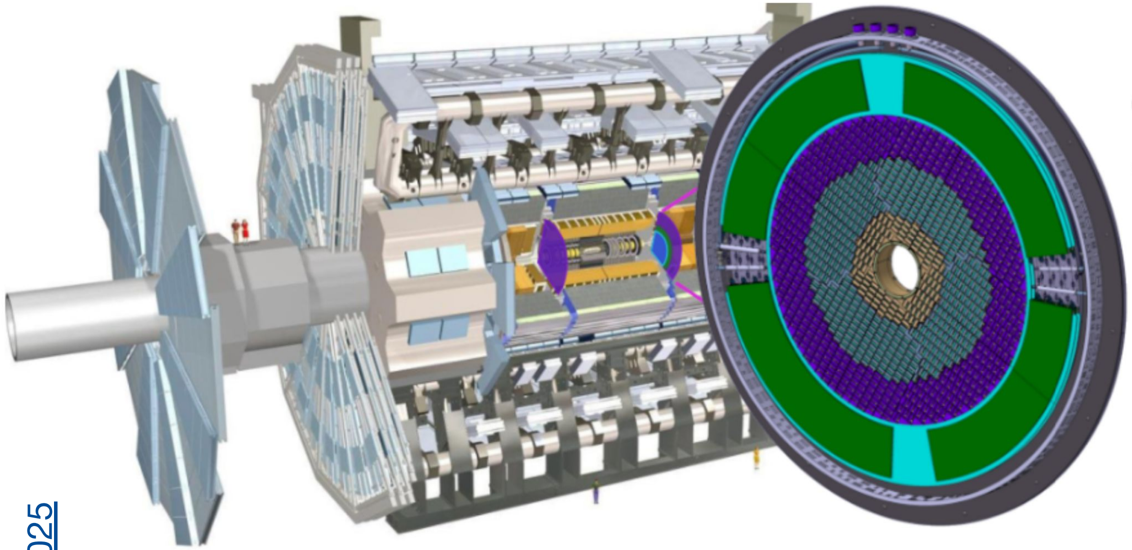


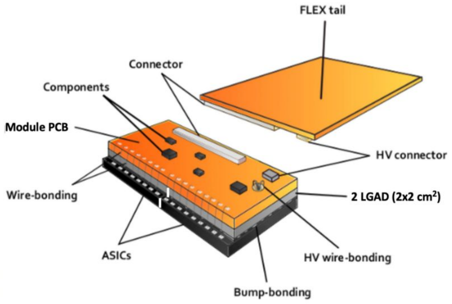


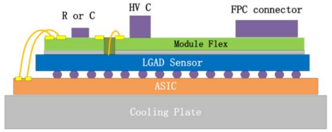
Courtesy of Paul Scherrer Institut

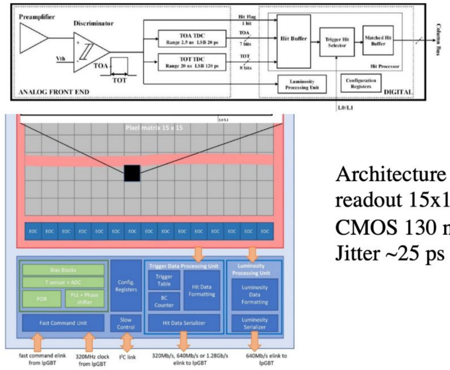
HL-LHC: First generation timing detectors

ATLAS High Granularity Timing Detector









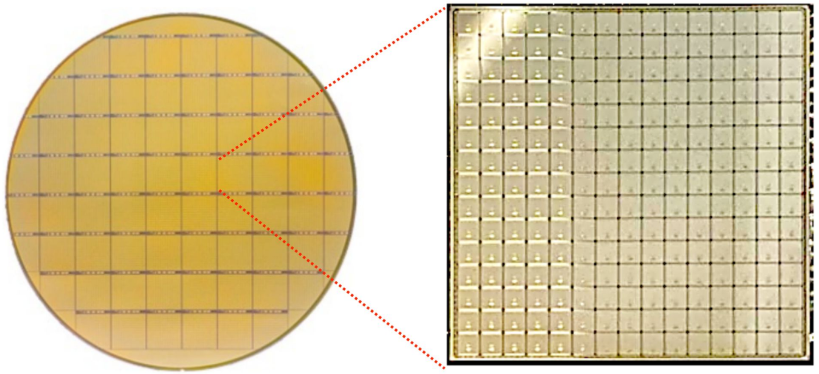
Architecture of the ALTIROC ASIC readout 15x15 pads, 2x2 cm^2, CMOS 130 nm, Jitter ~25 ps

Xiao Yang at VCI2025

2x double-sided layers, based on **Low Gain Avalanche Detectors** (LGADs) and custom ASICs (ALTIROC)

- Target: **30-50 ps per track** (35 - 70 ps per hit),
- **6.4 m²** silicon detector, **3.6M** channels, **1.3 × 1.3 mm²** pixel size, **50 μm** active thickness.

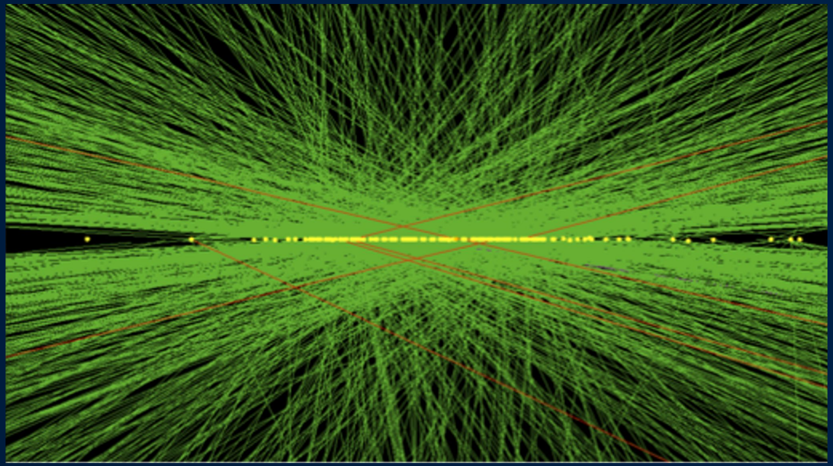
Radiation hardness requirement:
2.0 MGy TID and **2.5E15 n$_{eq}$/cm^{-2}** @ -30 °C
for **50 ps** and **4 fC**

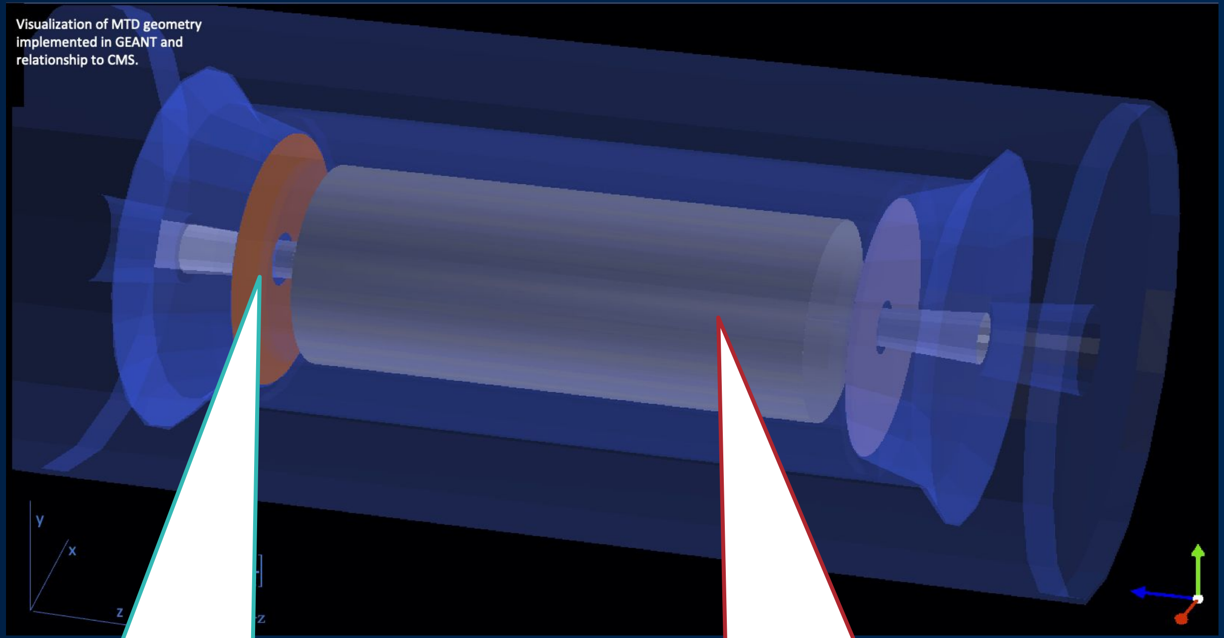


8-inch LGAD wafer   Full size 15*15 LGAD sensor

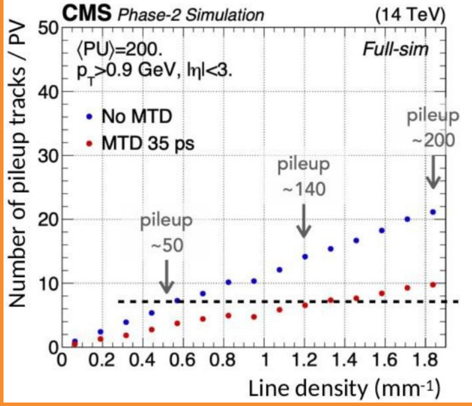
HL-LHC: First generation timing detectors

CMS Minimum Ionizing Particle Timing Detector





MIP Timing Detector (MTD) by CMS



The MTD will exploit timing information to reduce pile-up to current LHC level in both the forward and barrel regions.

Endcap Timing Layer (ETL)

Si with internal gain (LGAD):

- On the CE nose: $1.6 < |\eta| < 3.0$
- Radius: 315 < R < 1200 mm
- Position: z = ±3.0 m
- 1.3x1.3 mm^2 pixels
- ~14 m^2: 8.5M channels
- Fluence: up to 2E15 neq/cm^2

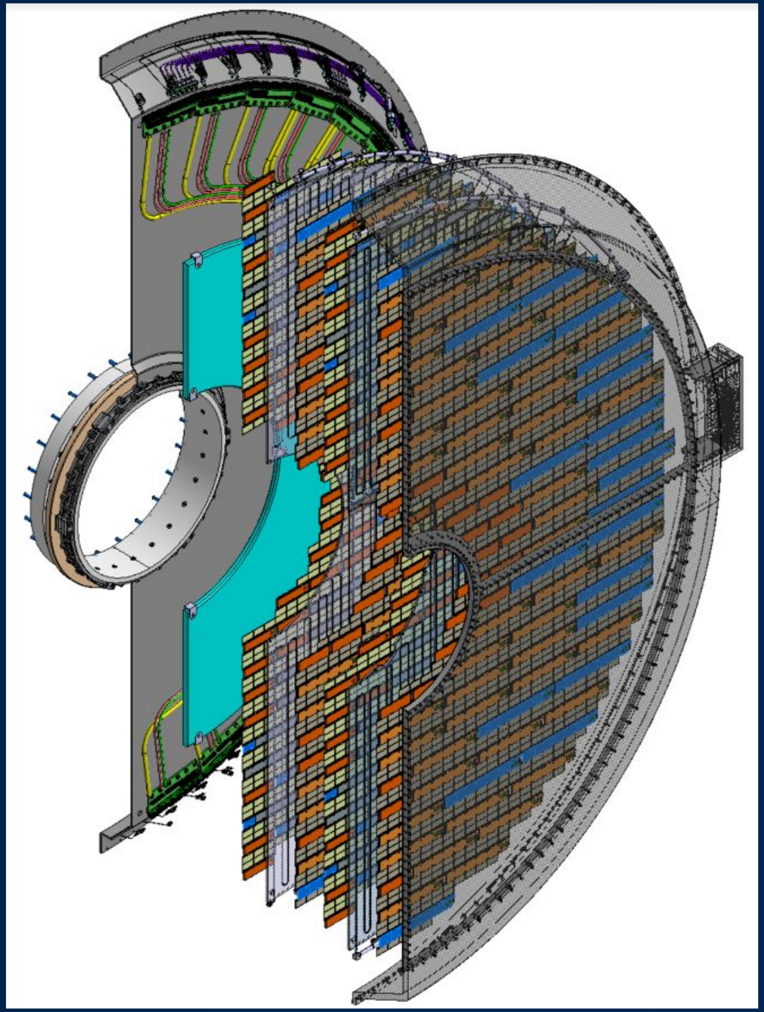
Barrel Timing Layer (BTL)

LYSO bars + SiPM readout:

- TK/ECAL interface: $|\eta| < 1.45$
- Inner radius: 1148 mm
- Thickness: 40 mm
- Length: ±2.6 m along z
- Area: 38 m2
- 332k channels

CMS Endcap Timing Layer

315 < R < 1200 mm, z = ±3.0 m, 1.6 < $|\eta|$<3.0, 1.3mm pixels, 14 m^2: 8.5M channels



More on the LGADs for the CMD ETL

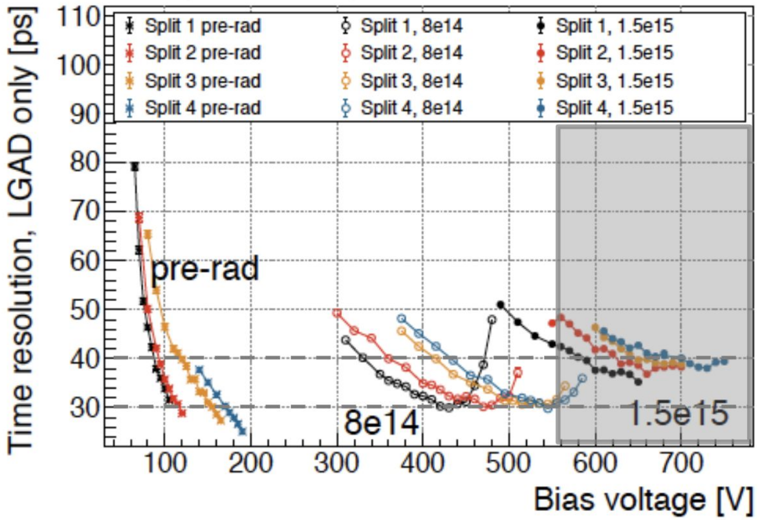
Design Constraints from the CMS MTD

Need to withstand 2 x 10^{15} n_{eq}/cm^2 in the innermost region over 3 ab^{-1}, still deliver 8-10fC for readout at the end of life

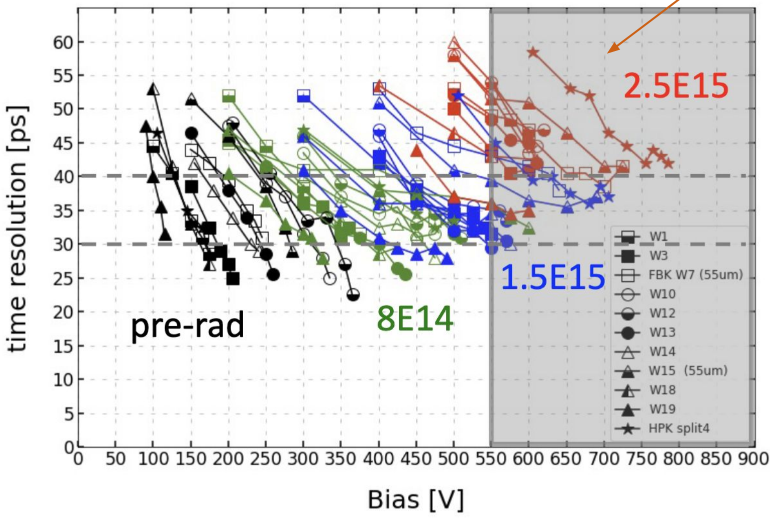
< 30-50 ps contribution from the sensor, limits active depth to 50um with a gain of 10-30 and pad size ~ mm^2 to minimize pad capacitance

V Sola at FAST2025

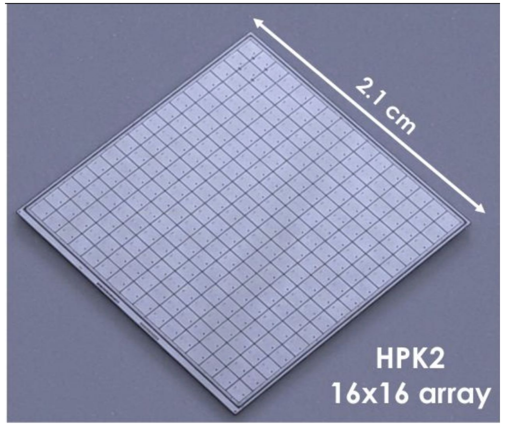
HPK2 – Beta source

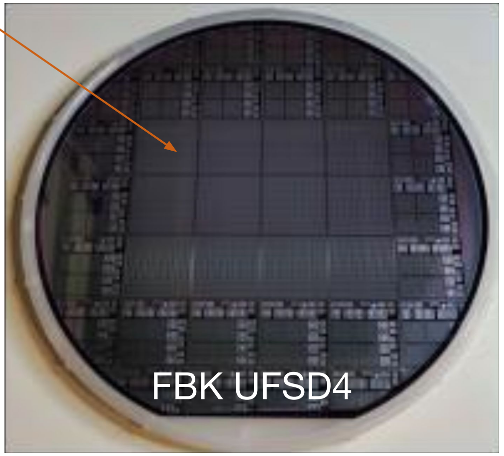


FBK UFSD3.2 – Beta source



Carbon Co-implants in Gain Volume





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More on the LGADs for the CMD ETL

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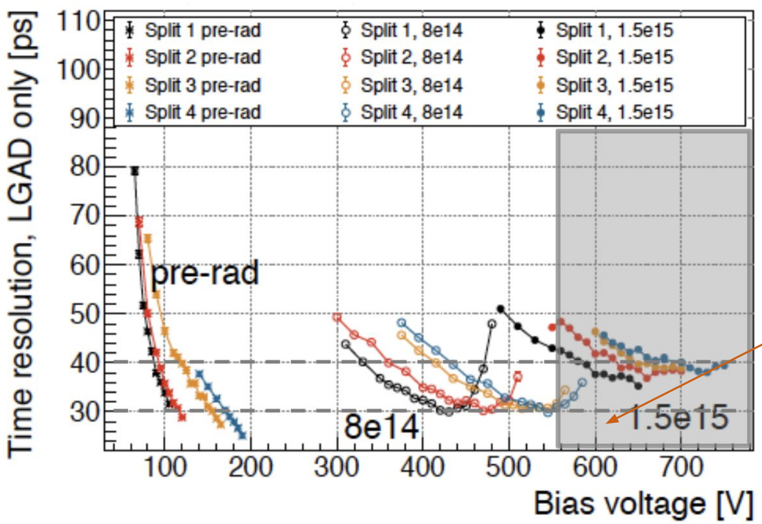

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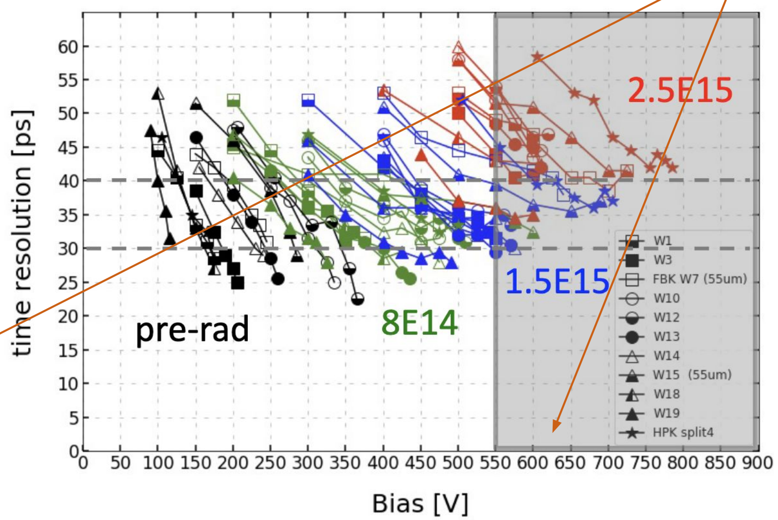

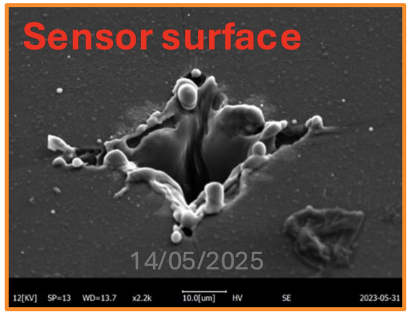

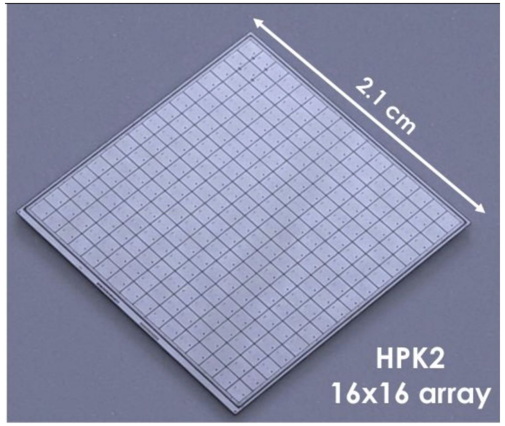

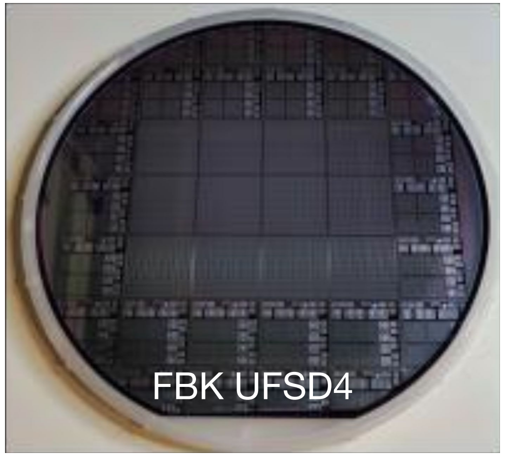

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Sensors for timing at Muon Colliders

- Positional Resolution of a few um
  a. Can be achieved without charge sharing with small pixels and staggered layers
     i. (p/2)/√12
  b. Easier to reach with charge sharing and larger pixels
- Temporal Resolution of ~20 ps
  a. Required for effective occupancy ~1%
  b. Has been achieved in several designs
- Pixel pitch down to 25 um
  a. Required for effective occupancy ~1%
  b. Standard LGADs face fill factor challenge due to field stops
- Good fundamental properties
  a. Uniform fields through the pixels
  b. Fast rise times and low noise
  c. Fast reset time due to constant influx of BIB
- Radiation Hardness
  a. HL-LHC levels of exposure at $10^{15}\ n_{eq}/cm^2$
  b. Ensure BIB exposure doesn't degrade timing performance beyond acceptable signals
- System level integration complexity
  a. Minimizing cross-talk and coupling
- Keeping the material as low as possible

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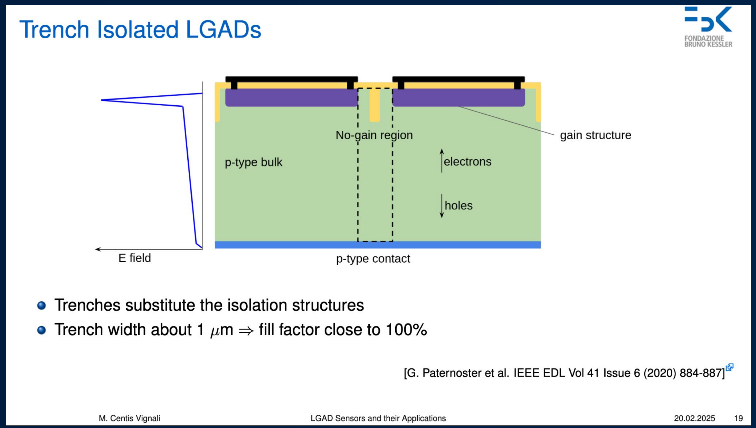
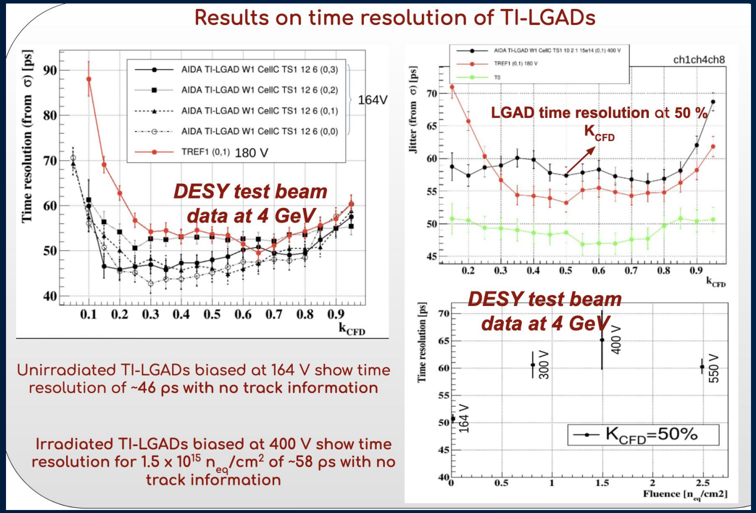
Recent talks highlighting latest developments

Trench Isolated LGADs

M C Vignali at VCI2025

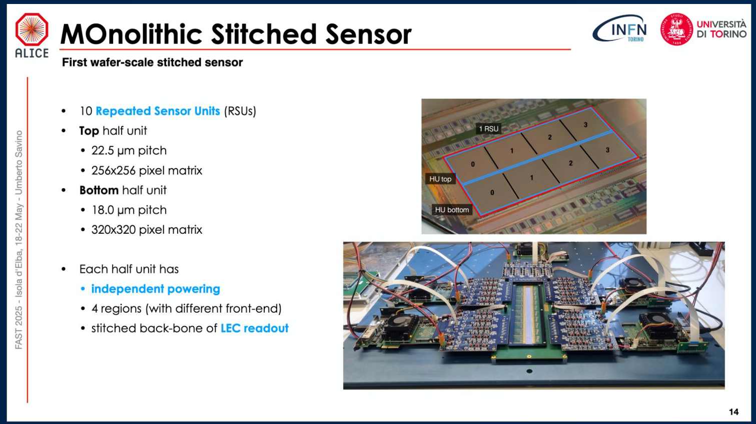


I Velkovska at TRENTO2025

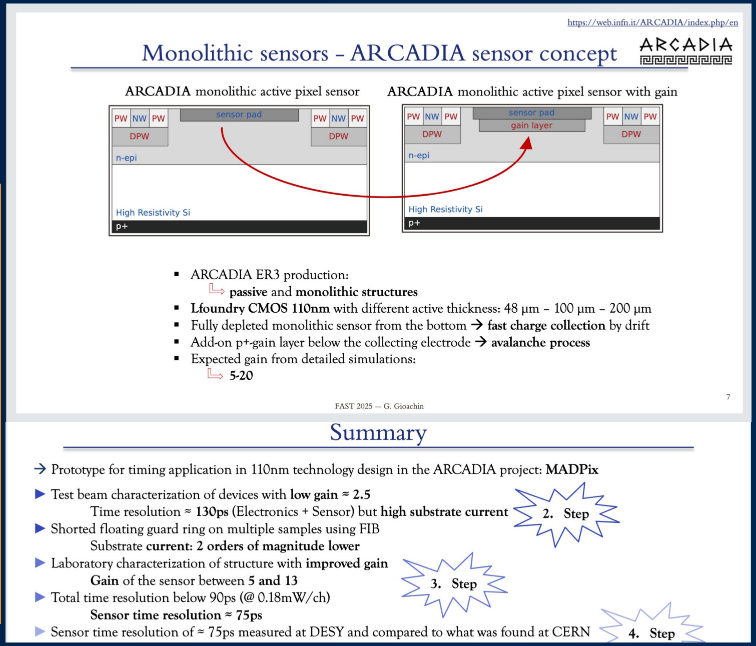


Monolithic Active Pixels

U Savino at FAST2025



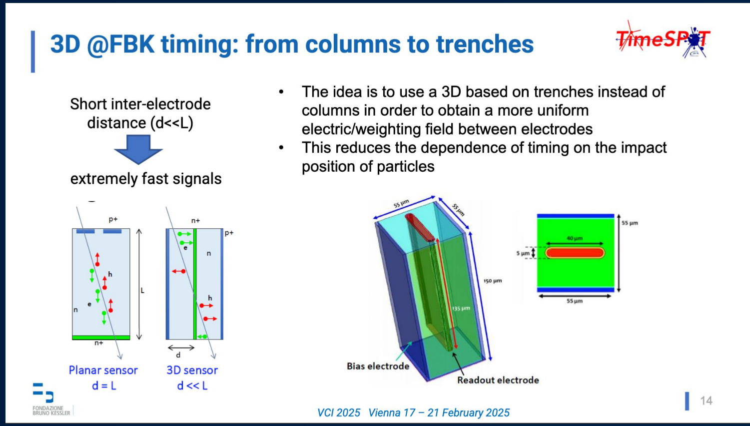
G Gioachin at FAST2025



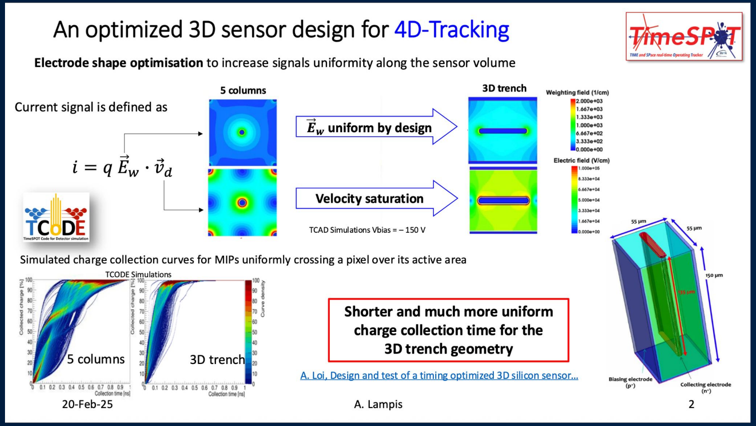
Recent talks highlighting latest developments

3D Sensors

M Boscardin at VCI 2025

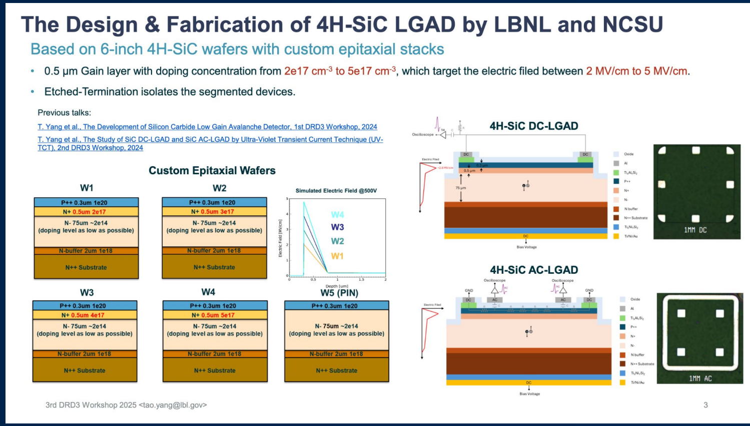


A Lampis at VCI2025

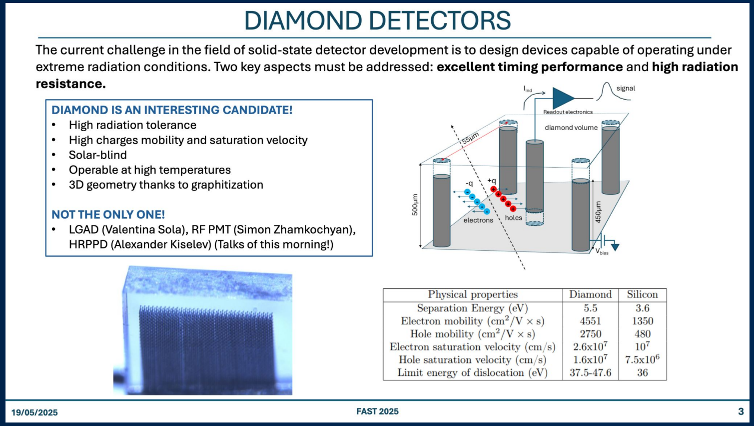


Diamond, 4H-SiC, etc

T Yang at DRD3 Week2025

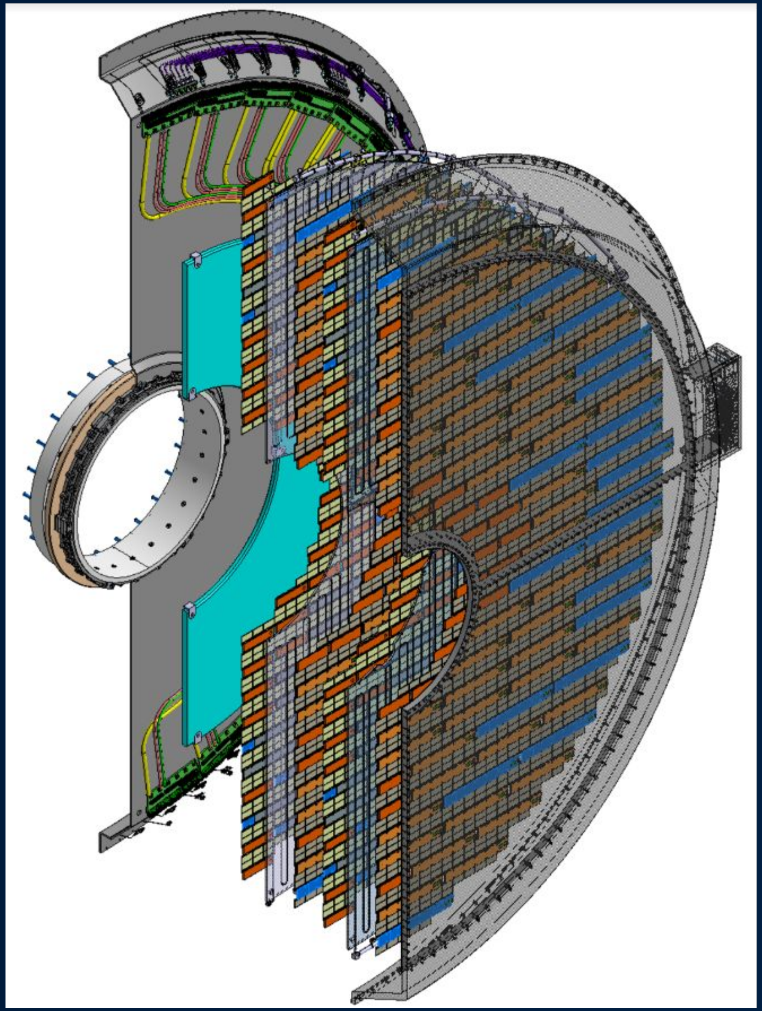


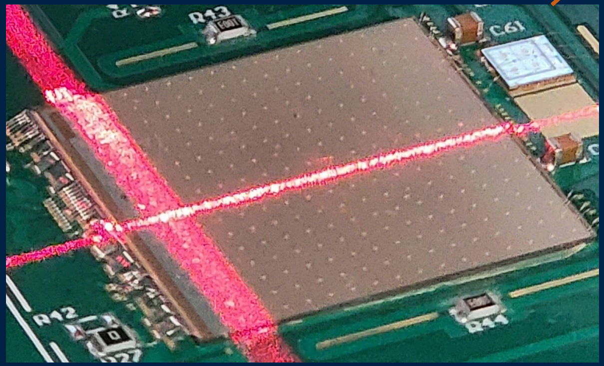
C Buti at FAST2025



CMS Endcap Timing Layer

~33k chips, 2.3 x 2.1cm chips, 1.3 mm pixels, 16x16 px





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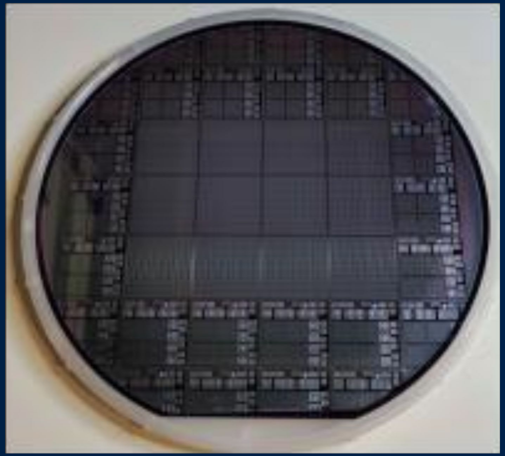
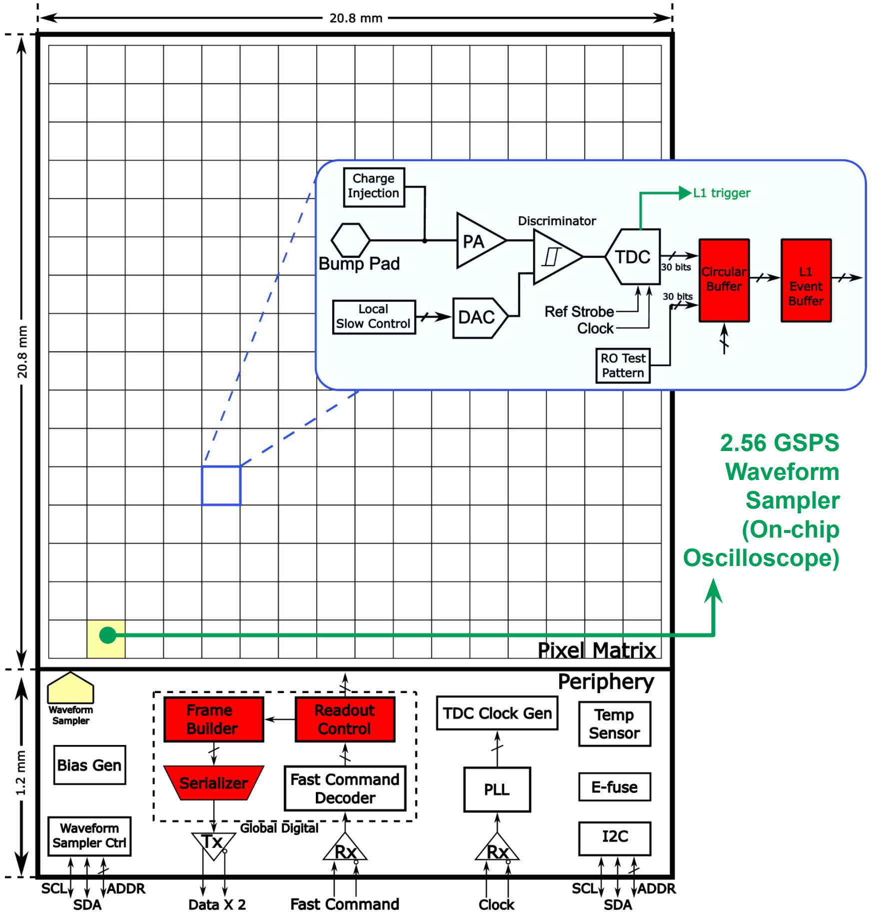


ETL Read Out Chip (ETROC)



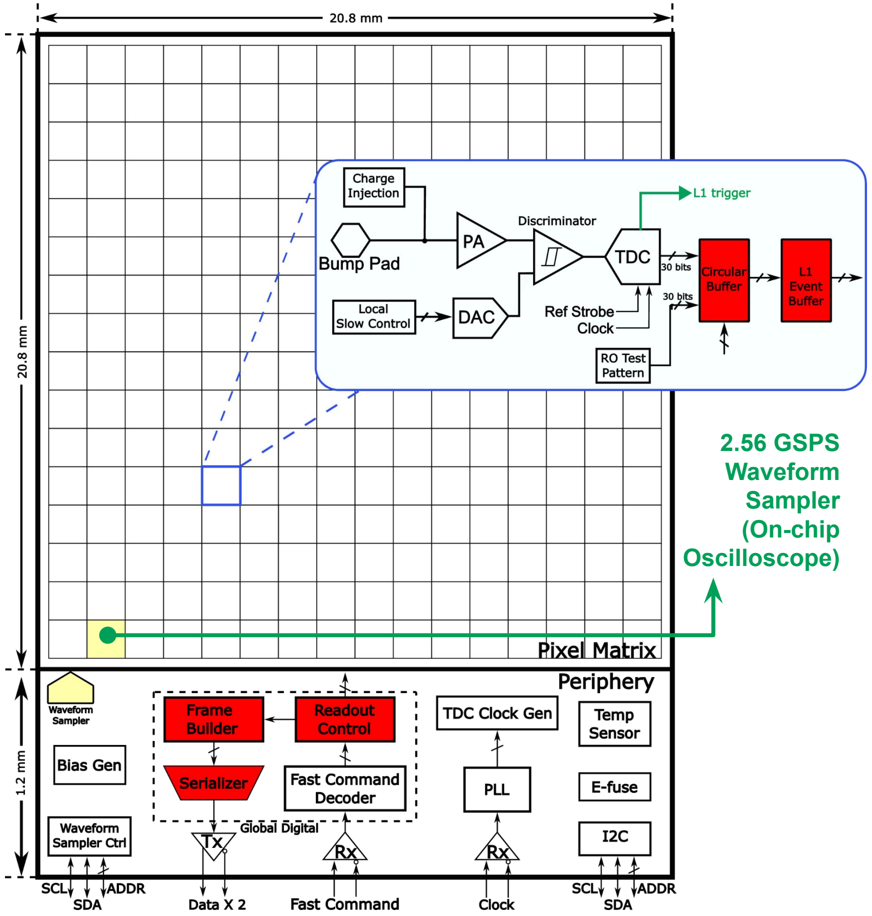
CMS Endcap Timing Layer

2 hits per track, 50ps res. per hit, 35ps res. per track

What are the main constraints on this design?

1. Low Noise
   - This is crucial! 30ps intrinsic (Landau) resolution from LGADs also **limits ASIC contribution < 40ps**
2. Low Power
   - Thou shall not fry your detector! Cooling capacity limits power consumption to **< 1W per chip, 4mW per pixel, 240mW/cm^2**
3. Radiation Hardness
   - Must withstand 100MRad over the 3000fb^{-1} of HL-LHC
4. Sensitive to small LGAD signals
   - Around 10fC per MIP towards end of lifetime of LGADs in ETL
5. Synchronized precision timing over ~33k chips, ~8.5M channels...

ETL Read Out Chip (ETROC)



CMS ETROC

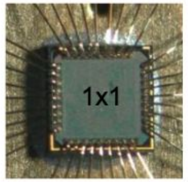
Long Journey to the full sized chip…

Sept 2018 | Dec 2018 | May 2019 | Aug 2019 | March 2020 | May 2020 | July 2021 | Sept 2021 …

Covid

Project started

ETROC0[1] submitted



Preamp + discriminator

AFE 1.6 - 2.4mW / px

ETROC1[2] submitted

Preamp + discriminator + TDC
4x4 H-tree clock distribution

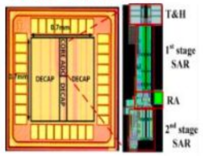
AFE 1.6 - 2.4mW / px
TDC 0.1mW / px

ETROC2: 8x8 → 16x16

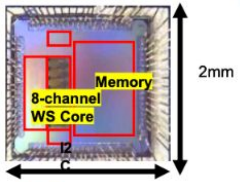
Decision to go for full size full functionality ETROC2,
Delay submission and add few test chips …

Total of 7 small chips, all successful

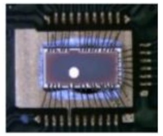
Single channel ADC submitted



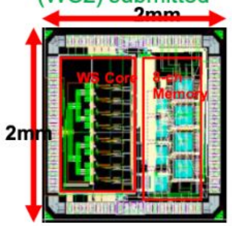
8-channel ADC Waveform Sampler (WS1) submitted



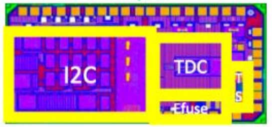
ETROC-PLL mini ASIC submitted



Rad-hard version of Waveform Sampler (WS2) submitted



I2C Test chip submitted

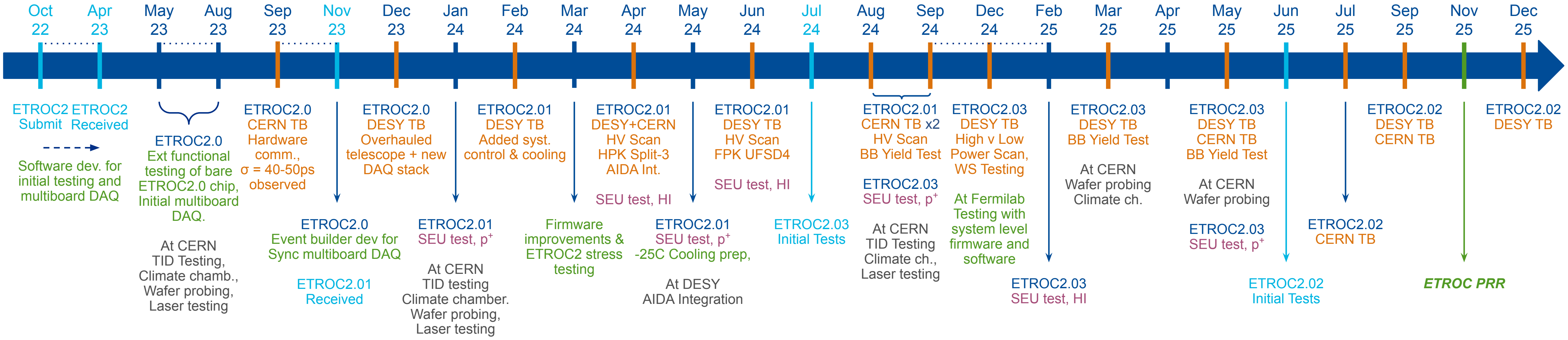


All analog blocks have been silicon proven in test chips;
ETROC2 FPGA emulator: has verified digital readout and system interfaces

Design team: FNAL/SMU/LBNL/UCSB
Testing team: FNAL/SMU/UIC/UCSB/Lisbon/IFCA/KUL with students from KSU/KU

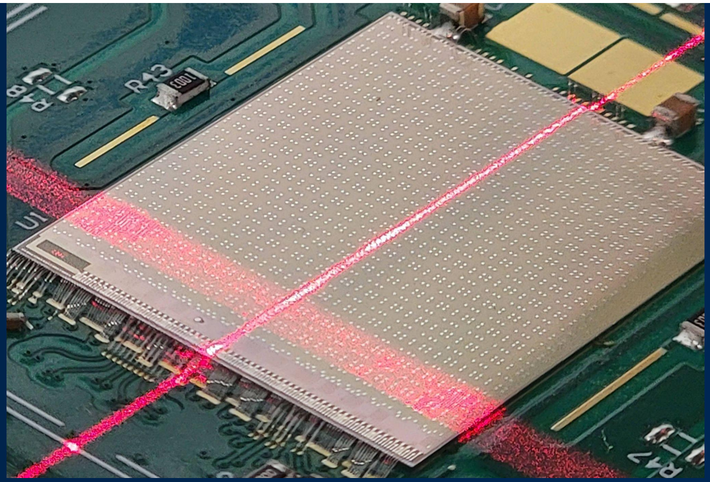
CMS ETROC

Extensive Characterization Campaign with the full sized ETROC2 chip

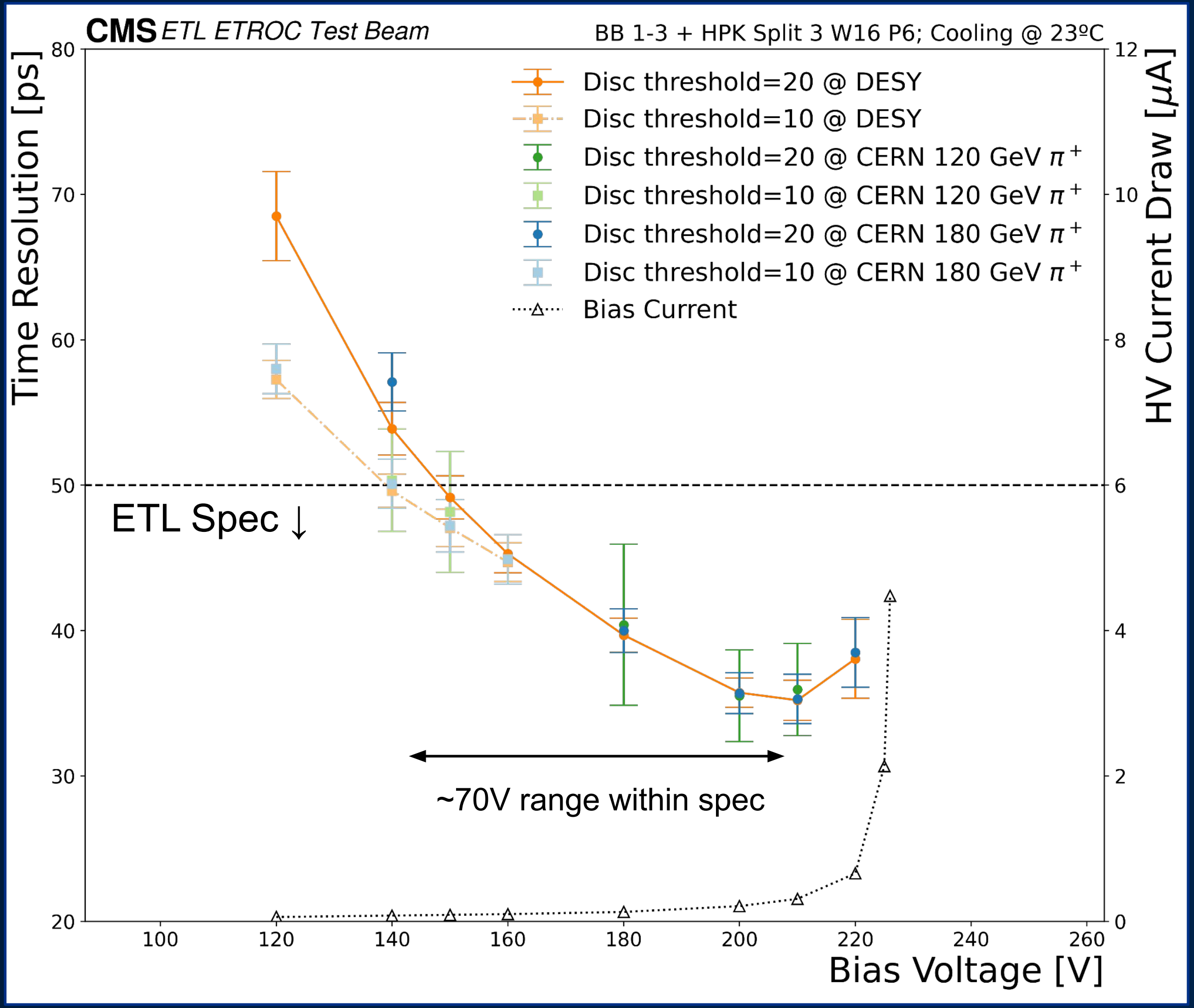


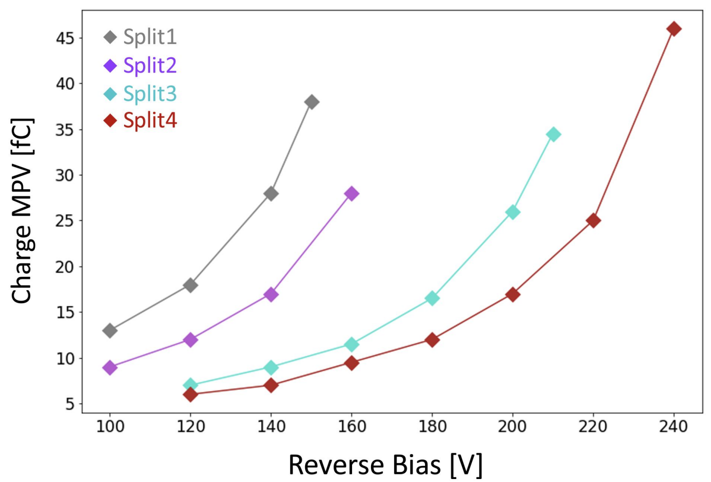
Takes a long time to validate the performance of a precision timing chip, often involving a very heterogeneous testing campaign

ASIC design must also incorporate elements of the full system hybridization, and must have flexibility to adapt to design modifications



CMS ETROC2 Performance





Sensor under consideration here is HPK2 **Split 3**

Successfully reproduced ~35ps res. *with this board. Results from CERN 120-180 GeV π^+ agree with those from DESY 4 GeV e^- beam*

Total typical chip power consumption is below 800 mW, well within the design constraints on the ETROC

ASICs for timing at Muon Colliders

- Scaling of TDC Performance with Smaller Technology Nodes
  a. Higher speed and lower power consumption at the transistor level, higher channel density
  b. Process variations, reduced voltage headroom, higher operating frequencies and jitter require new solutions for scalable timing detectors

- Power Density and Heat Dissipation
  a. Power Delivery Network will be a big challenge with smaller nodes and higher channel density
  b. Cooling! Current gen detectors have ~4mW/channel, which is orders of magnitude more than trackers at ~10uW/channel.

- Radiation Hardness

- Increased Complexity and Integration
  a. Design and verification will be trickier.
  b. Interconnect and routing more difficult with signal integrity and routing congestion

- Development cost and yield for smaller and more cutting edge nodes

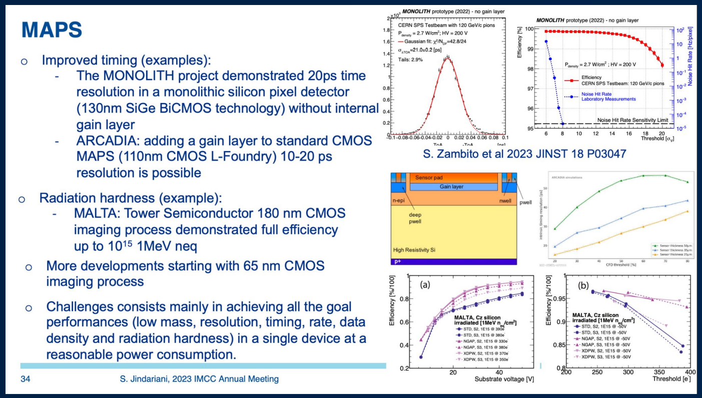
- System level integration complexity
  a. Precision clock distribution
  b. Power distribution
  c. Minimizing cross-talk and coupling

- Streaming Model for DAQ?

Selection of past talks highlighting latest developments

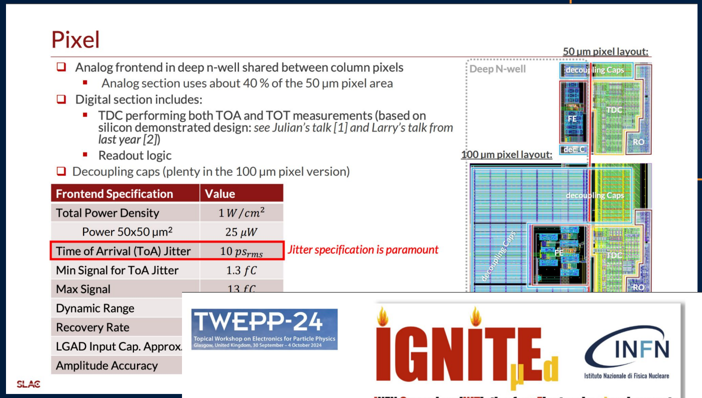
MAPS

Sergo Jindariani



Smaller Nodes

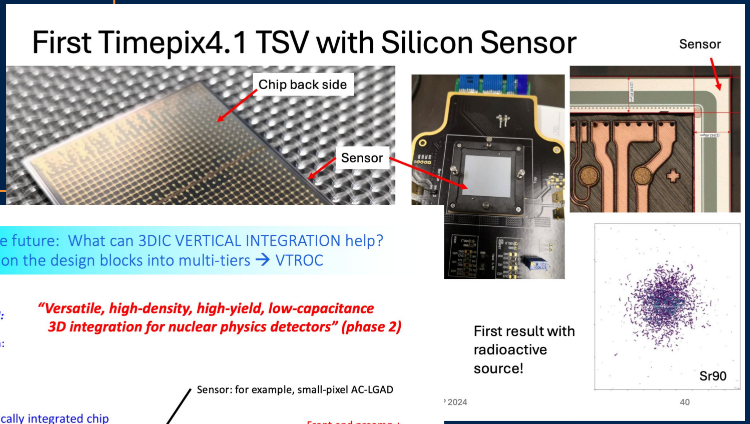
Bojan Markovic



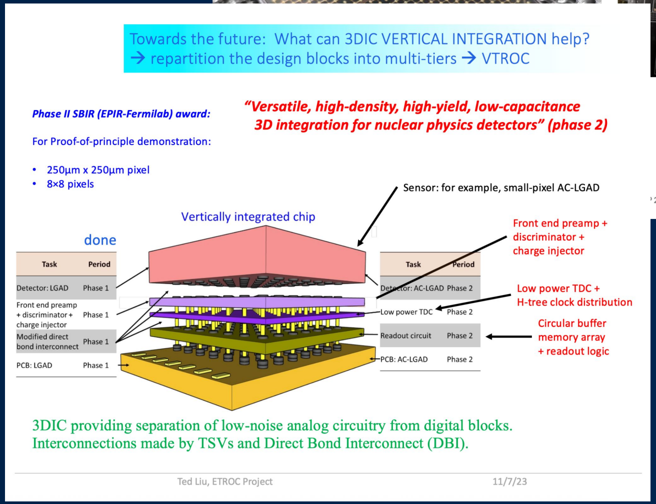
Gian M Cossu

3D Integration

Francisco P Diaz



Ted Liu



FERMI NATIONAL ACCELERATOR LABORATORY

Is this where the future lives?

MAPS

Sergo Jindariani

- Minimizing signal path length and parasitic capacitance at the pixel level.
- Small signal amplitudes easier to deal with optimized analog front-end design tightly integrated with the sensor
- Integrating components and simplifying local power routing, less localized heat sources in this layer.

Smaller Nodes

Bojan Markovic

Gian M Cossu

- Reduce the power consumption per digital function, thereby lowering the overall heat generated by the most complex layers.
- Faster digital processing and higher clock speeds with improved power efficiency.
- May provide the transistor density and performance needed to implement sophisticated radiation-hardened digital logic and error correction schemes efficiently in terms of power and area.
- Possibly allows for more complex on-chip circuitry for advanced techniques, sophisticated power management, and clock management units within the digital layers, all while contributing to lower overall power.

3D Integration

Francisco P Diaz

Ted Liu

- Efficient heat removal pathways (microchannels or thermal vias) closer to or in between the heat sources.
- Shorter, lower-impedance power and ground paths through the stack. Shorter, more direct clock routing paths with reduced skew across the chip
- Stacking multiple layers of electronics vertically can help with footprint
- High data rates due to high-bandwidth, low-power vertical interconnects between layers.
- Possible noise reduction allowing physical separation and shielding between sensitive analog layers and noisy digital layers.

Fermilab

FermiFORWARD

U.S. DEPARTMENT of ENERGY

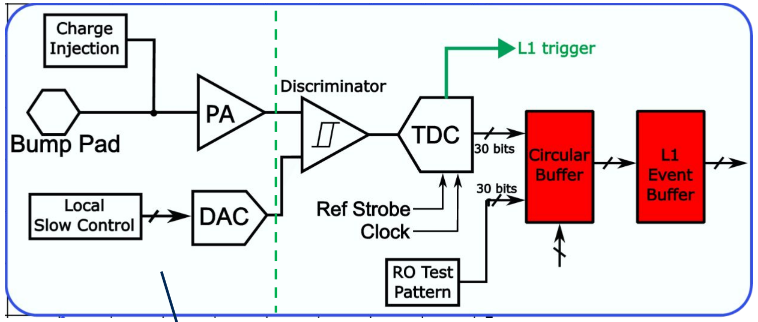
CMS ETROC Acknowledgments

- *This work was produced by FermiForward Discovery Group, LLC under Contract No. 89243024CSC000002 with the U.S. Department of Energy, Office of Science, Office of High Energy Physics. Publisher acknowledges the U.S. Government license to provide public access under the DOE Public Access Plan DOE Public Access Plan*

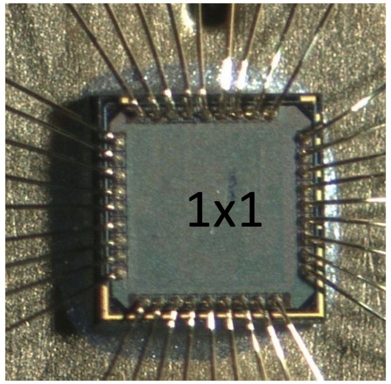
- *The measurements leading to these results have been performed at the Test Beam Facility at DESY Hamburg (Germany), a member of the Helmholtz Association (HGF).*

- *The research leading to these results has received funding from the European Union's Horizon Europe research and innovation programme under grant agreement no. 101057511.*

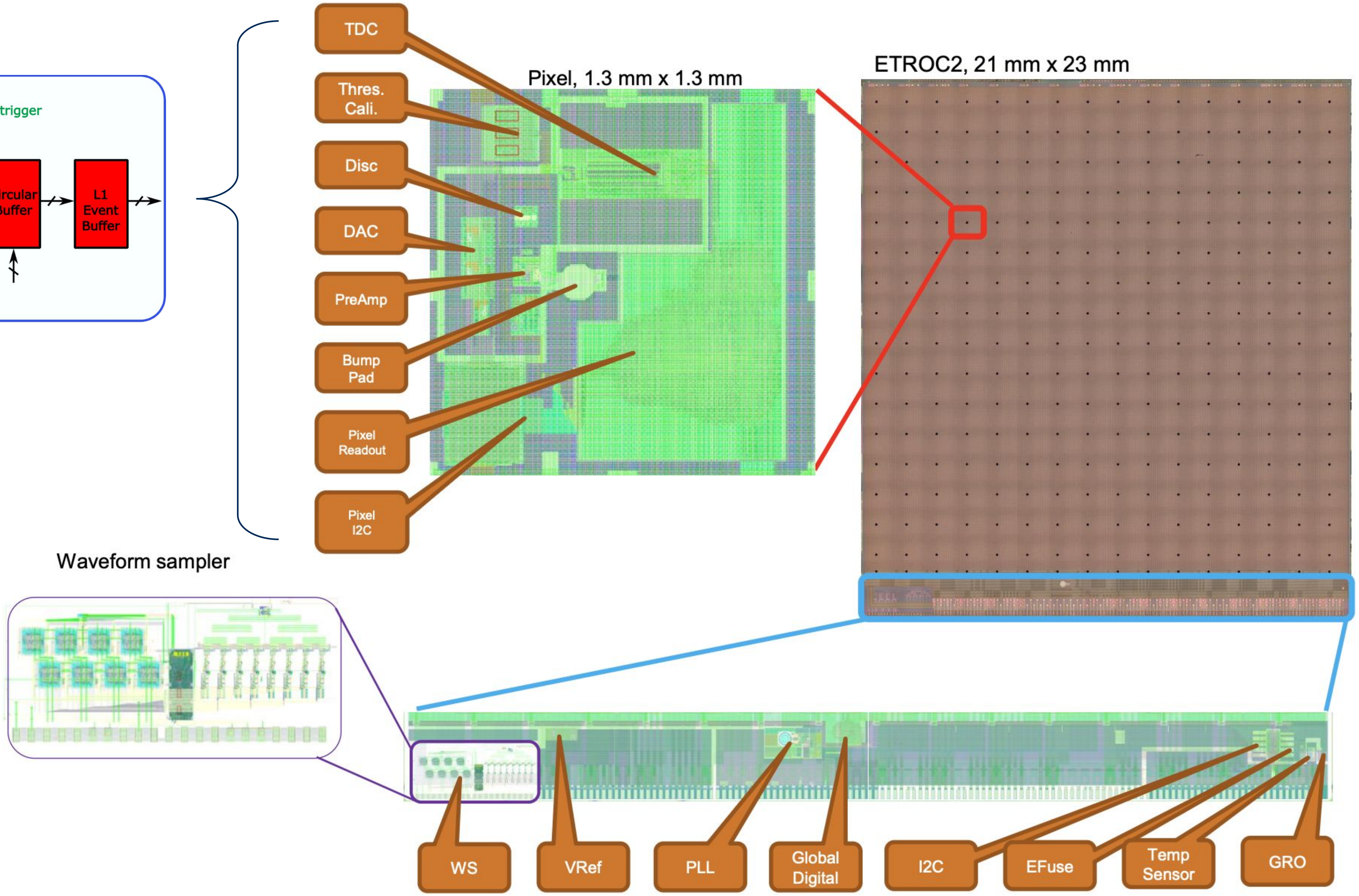
CMS ETROC



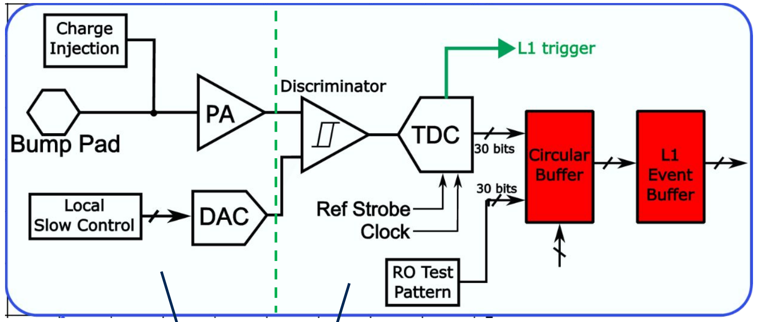
Dec 2018
ETROC0 submitted



AFE 1.6 - 2.4mW / px

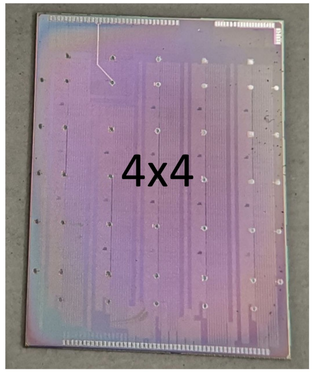


CMS ETROC



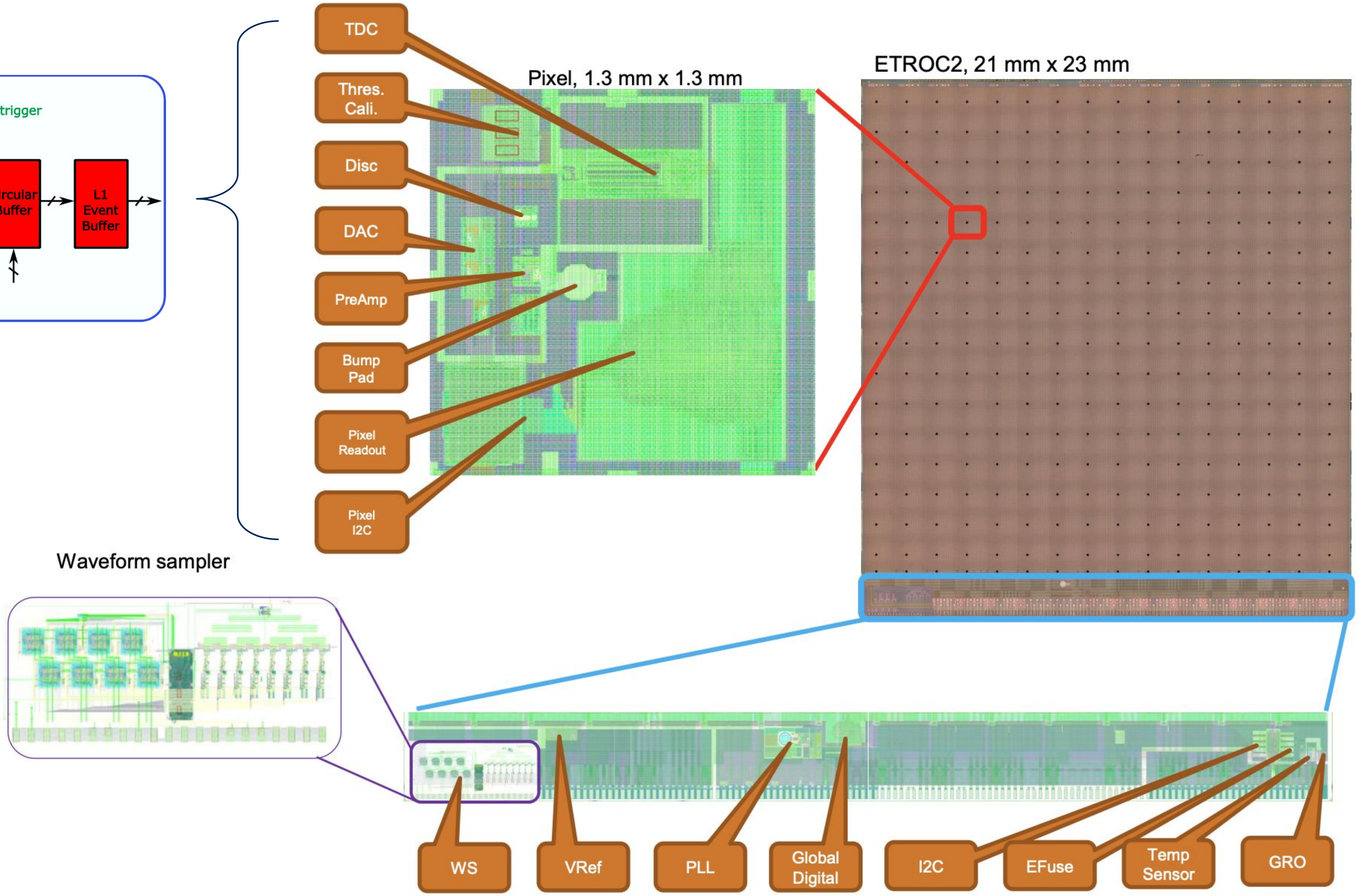
Aug 2019

ETROC1 submitted

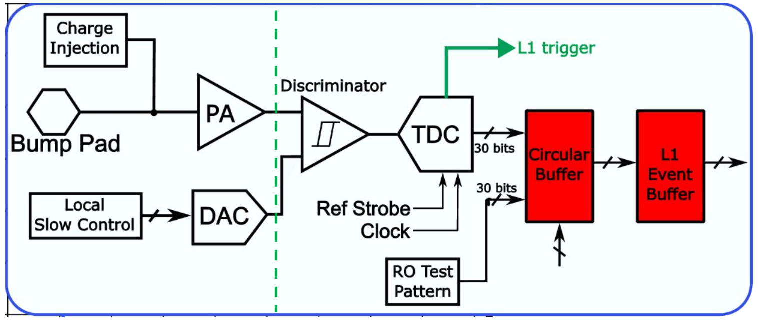


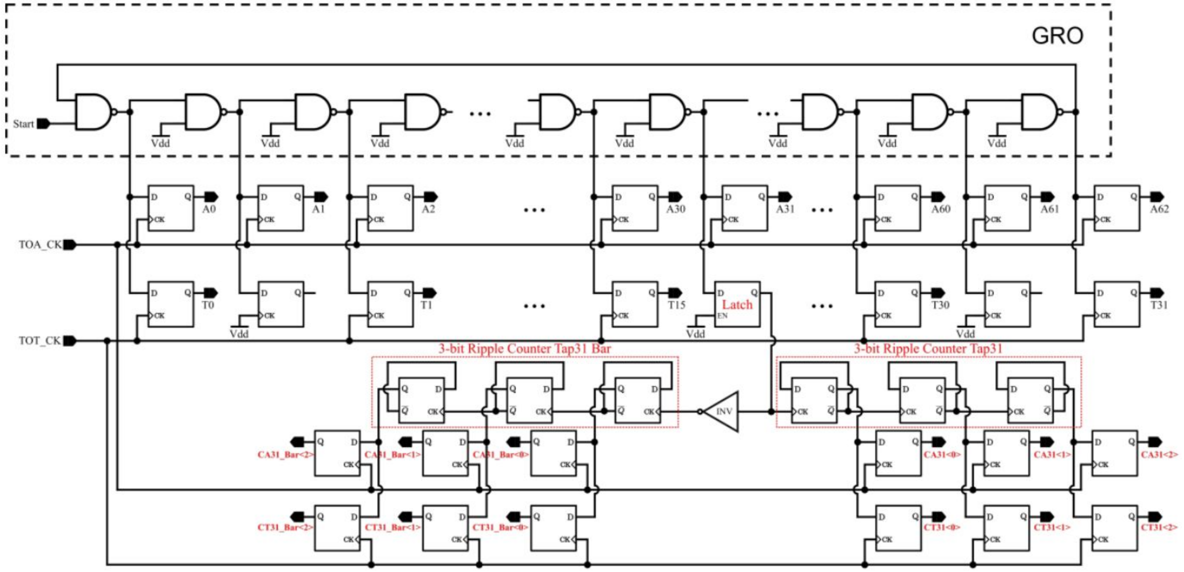
AFE 1.6 - 2.4mW / px

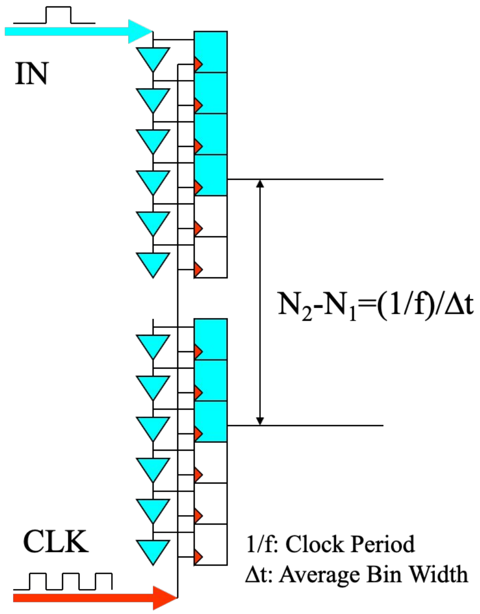
TDC 0.1mW / px



CMS ETROC - TDC Design







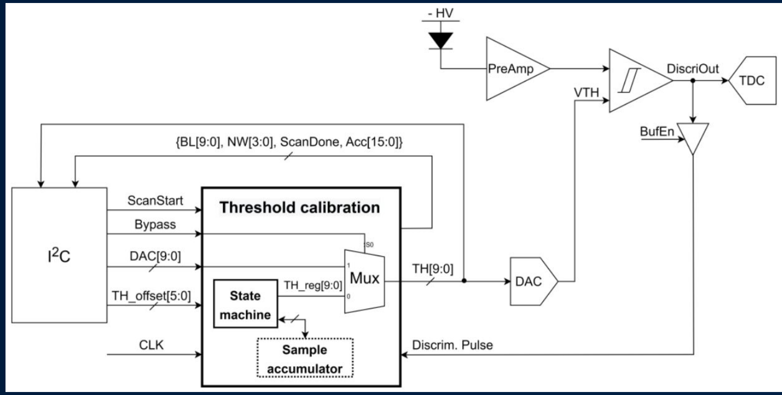
Several design features aimed at reducing power compunstion and complexity while retaining good performance

- Delay line based TDC with uncontrolled delay cells
- PVT Effects calibrated with Self-Calibration scheme
- TOA bin size ~ 18ps, TOT bin size ~ 36ps
- Power Consumption limited to 0.1mW at 1% occupancy

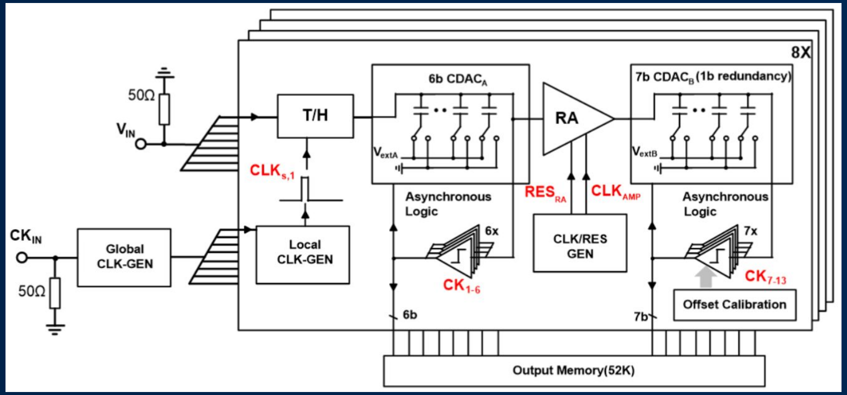
ETROC - Beyond The Timing Precision

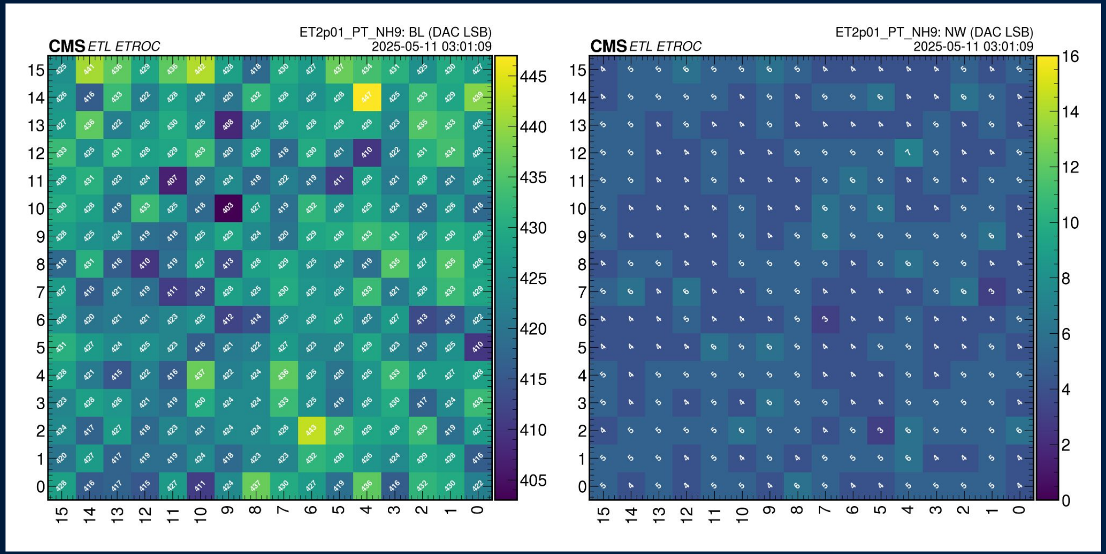
ASIC Design must incorporate features that make the detector operation feasible

Automatic Baseline Calibration

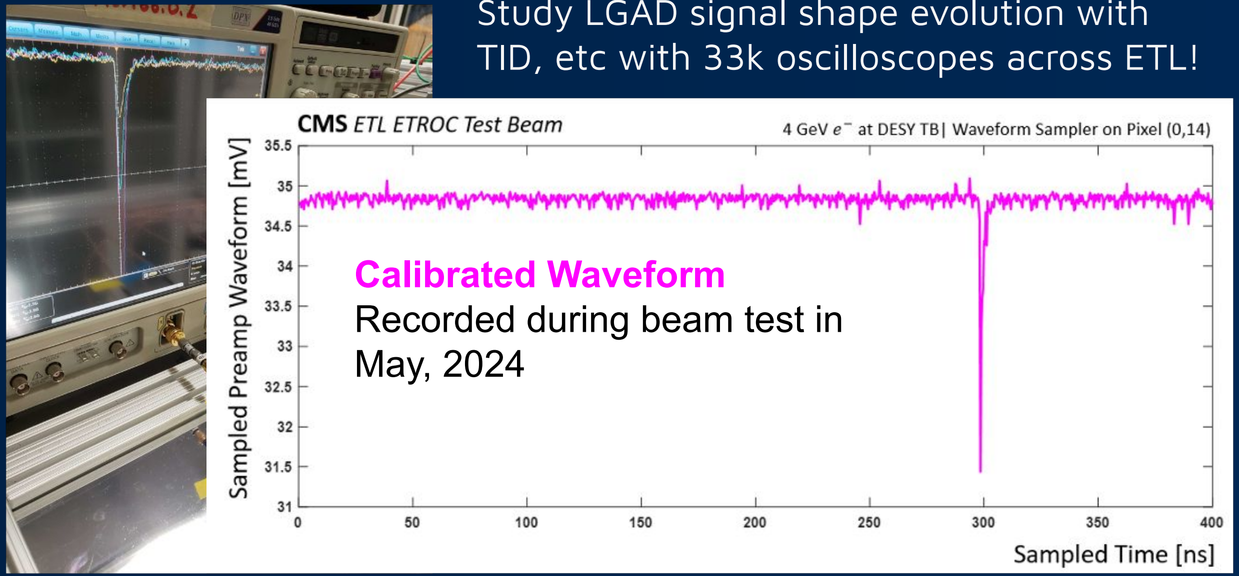


2.56GSps Waveform Sampler



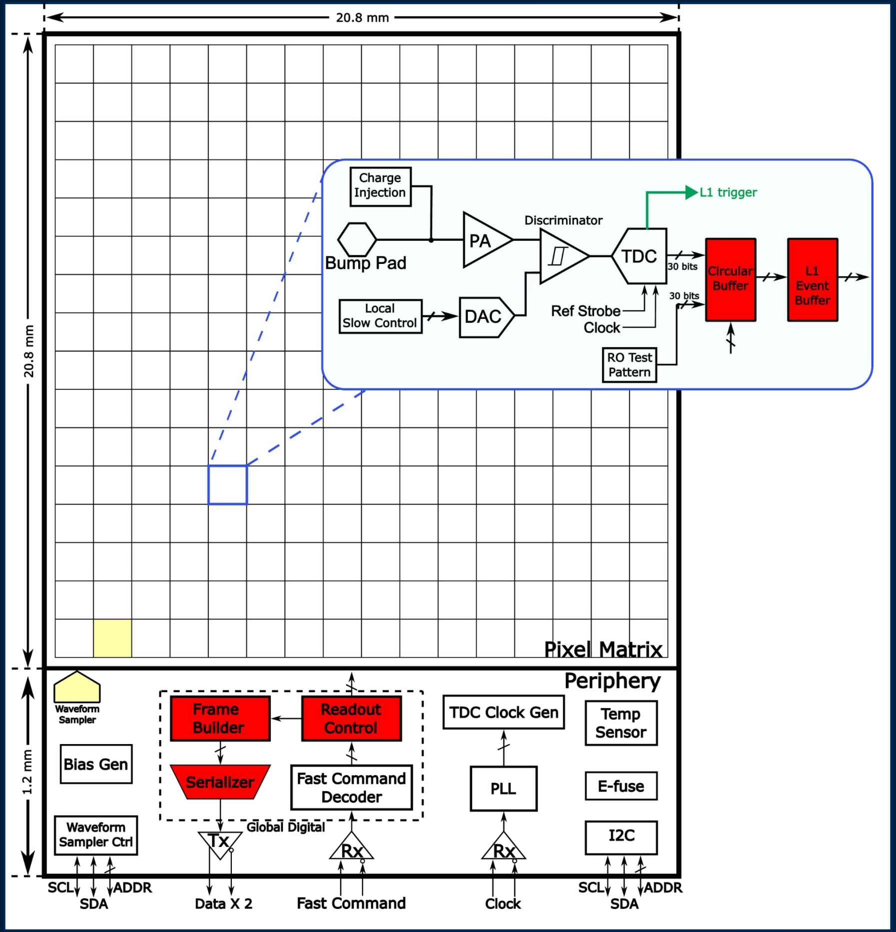


Study LGAD signal shape evolution with TID, etc with 33k oscilloscopes across ETL!



ETROC - Beyond The Timing Precision

ASIC Design must incorporate features that make the detector operation feasible



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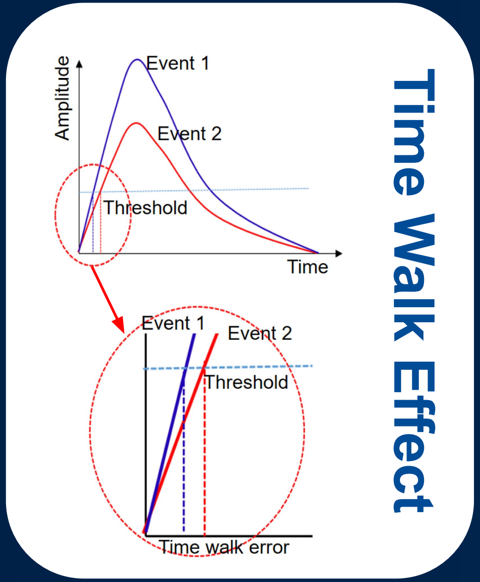

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256 Unique time walk correction parameters?

ETROC - Beyond The Timing Precision

ASIC Design must incorporate features that make the detector operation feasible

We only need 1 pixel's!

TDC Self-calibration with double strobe method helps eliminate PVT variations across the 16x16 array of pixels

This also means each of the 16x16 pixels is expected to perform identically once the self calibration is applied to each pixel