Testing the SmartPixels Prototype: Data Reduction with a Neural Network On-Chip

Daniel Abadjiev[1], Anthony Badea[1], Jennet Dickinson[2], Karri DiPetrillo[1], Mira Littmann[1], Benjamin Parpillon[3], Danush Shekar[4], Eric You[1] on behalf of Smartpixels Collaboration

[1]University of Chicago, [2]Cornell University, [3]Fermi National Accelerator Laboratory, [4]University of Illinois Chicago

Pixel Tracking at Particle Collider Experiments

- At particle accelerators, silicon pixel sensors track charged particles produced near the collision
- The high granularity and timing resolution leads to petabytes of data generated per second [1]
- At a 10 TeV muon collider, a high level of beam-induced background (BIB) would overwhelm physics signal, exceeding readout constraints
- On-detector machine learning can distinguish signal from BIB in order to enable tracker readout

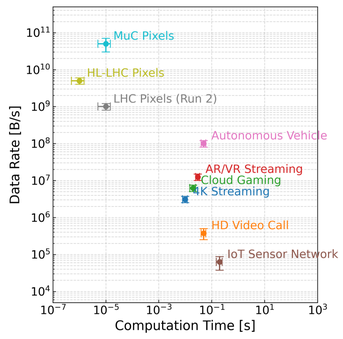

Figure 1: Approximate data rate of pixels at a muon collider and the LHC compared to commercial applications.

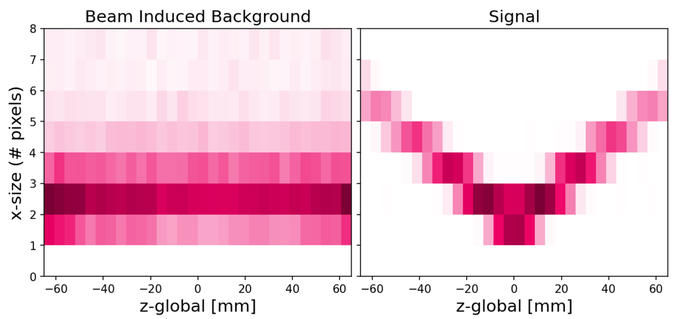

Figure 2: Simulated distributions of the size of clusters from beam induced background (left) and signal (right) in a pixel detector at a 10TeV muon collider.

Smartpixels: Neural Network on an ASIC

- High radiation, power constraints, and latency require the use of Application Specific Integrated Circuits (ASIC) to read out pixels
- The smartpixels project puts a neural network implemented with digital logic in silicon onto an ASIC to perform data compression and reduction on-detector

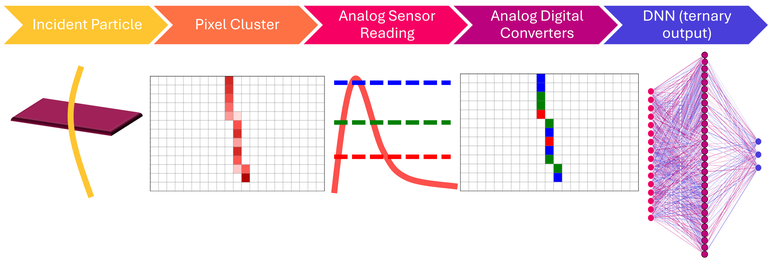

Figure 3: Cartoon schematic of a prototype smartpixel ASIC. Charged particles produce analog signals in a pixel cluster, which are digitized by a 2-bit ADC, and then the sums of each pixel row proceed into a classifier neural network with a ternary output.

Testbench for Prototype Smartpixel ASIC

- Test stands developed at Fermilab, and replicated at University of Chicago and Cornell University, are being used to evaluate a prototype ASIC
  - Based on open-source Caribou testing platform
- A workstation runs spacely (python program), which communicates with peary (C++ program) running on a ZCU102 board with an integrated field programmable gate array (FPGA)
- The FPGA and ASIC communicate through a Control and Readout (CaR) board and a custom ASIC board (Figure 4)
- A function generator is used for injecting charge into the ASIC board to simulate pixel sensor readout.

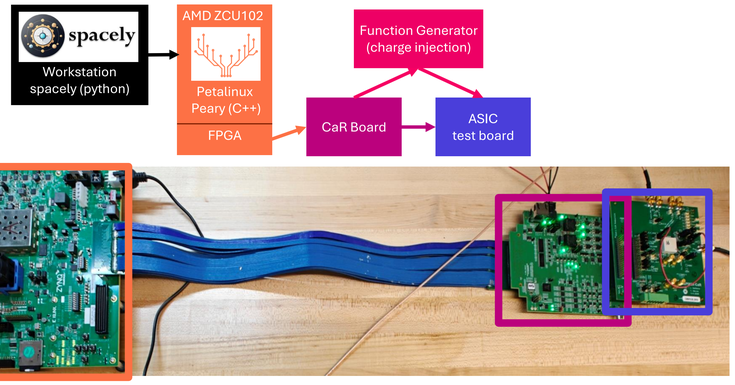

Figure 4: Flowchart of testbench for ASIC testing (top) and picture of University test stand (bottom). The workstation communicates with ZCU102 via ethernet. The FPGA on the ZCU102 is connected to the CaR board, which plugs into a custom ASIC test board.

S-Curve Noise Measurement

- To characterize analog component of the prototype ASIC, a varying amount of charge was injected while measuring the likelihood of a bit as 0 or 1, hence generating an S-Curve for each bit
- S-Curves were measured for each of 3 thresholds for 256 pixels
- Fit to a normal cdf to extract per-pixel noise and turn-on voltage

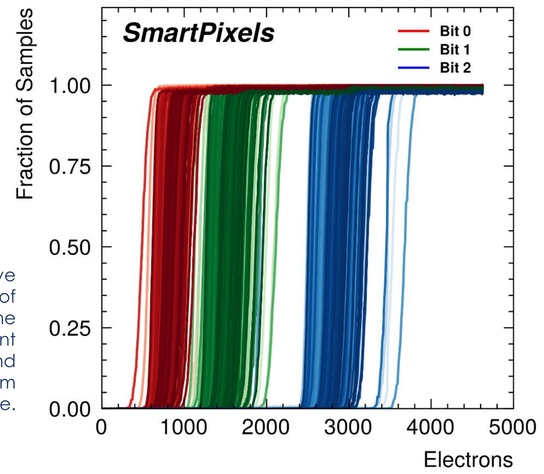

Figure 5: S-Curve measurement of the noise of the ASIC in the current test stand evaluated at room temperature.

Cold Testing

- At Fermilab, the ASIC test stand noise and the DNN performance were evaluated at room temperature
- At University of Chicago, the noise of the ASIC in the test stand was also measured at low temperature (-19 C).

	Bit Threshold (e^-)	Pixel Noise (e^-)
Bit 0, +20 C	840.9 ± 91.6	52.1 ± 5.6
Bit 0, -19 C	685.8 ± 50.1	36.8 ± 4.2
Bit 1, +20 C	1535.4 ± 114.3	48.5 ± 6.1
Bit 1, -19 C	1320.3 ± 66.4	36.6 ± 3.9
Bit 2, +20 C	2885.9 ± 145.6	48.7 ± 6.2
Bit 2, -19 C	2592.4 ± 91.2	38.2 ± 2.9

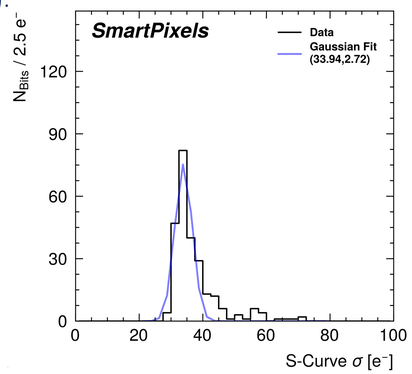

Figure 6: Noise distribution of 256 pixels measured at room temperature and about -19 C, extracted from fitting the S-Curves to a normal cdf (left). Sample distribution of noise in bit 0, measured at -19 C (right).

DNN Performance

- DNN performance was tested at Fermilab to compare the on-chip performance to a simulated model classifying pixel clusters as low momentum or high momentum.

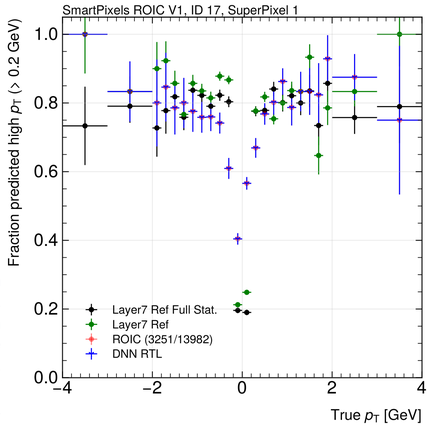

Figure 7: Performance of DNN in classifying momenta input clusters. Simulations of the model in python (green, black), simulation of the model on chip architecture (blue), and test-stand performance of DNN on-chip (red).

Future Work

- Implement DNN performance testing at university test stands
- Adapt on-chip DNN for use with a model that classifies pixel clusters as BIB or physics signal.
- Characterize impact of noise on DNN performance and reduce noise in ASIC design and in test stand

References

[1] Yoo, J., et al. "Smart pixel sensors: towards on-sensor filtering of pixel clusters with deep learning", *Machine Learning: Science and Technology*, vol. 5, no. 3, Art. no. 035047, IOP, 2024. doi:10.1088/2632-2153/ad6a00. https://arxiv.org/abs/2310.02474

[2] Dickinson, J., et al. "Smartpixels: Towards on-sensor inference of charged particle track parameters and uncertainties." , Dec. 2023. https://doi.org/10.48550/arXiv.2312.11676

Logos: Fermilab, Uchicago, USMCC, smartpixels

Work on behalf of https://fastmachinelearning.org/smart-pixels/